IBM®

Customer Engineering

Manual of Instruction

7503 Card Reader

7614 Reader Control

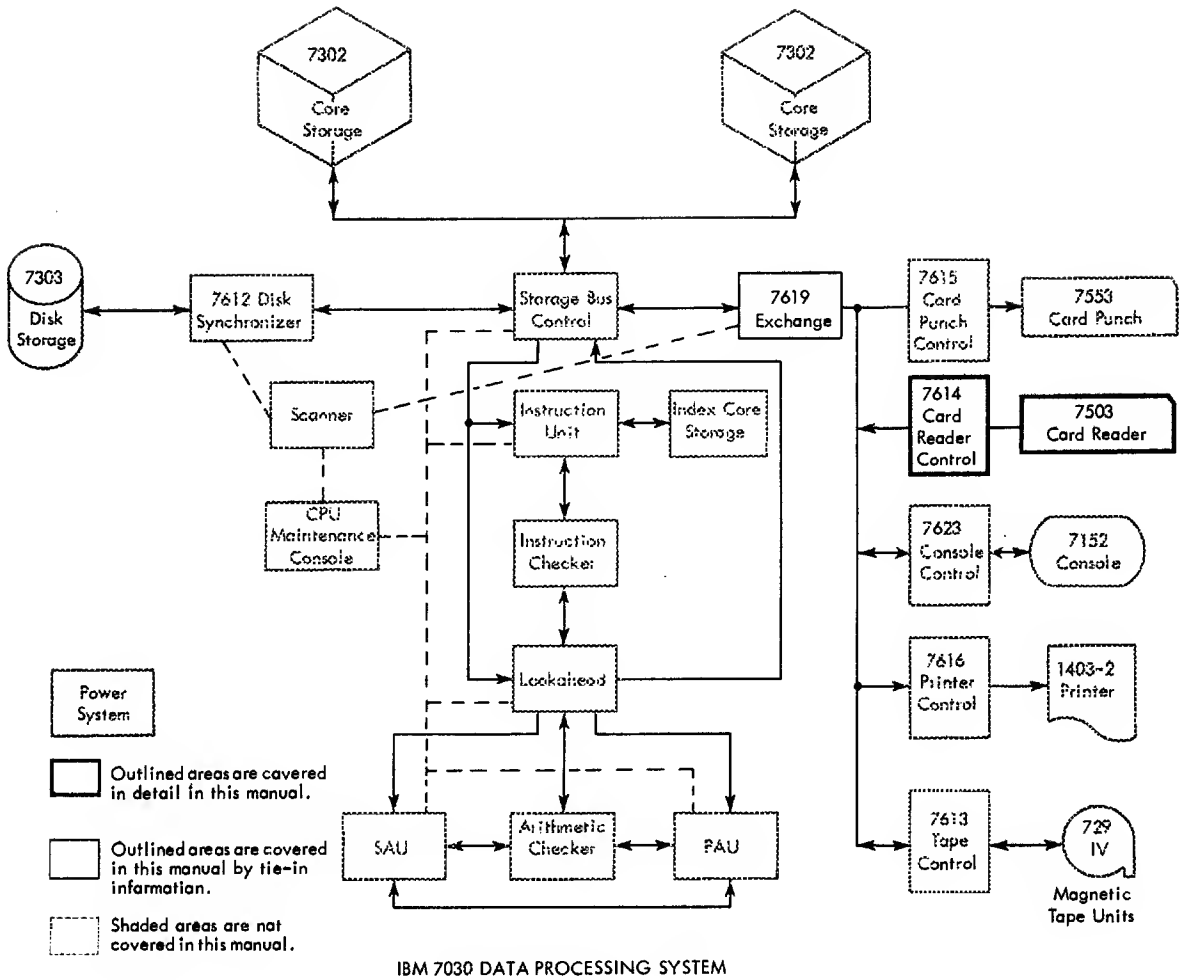
PREFACE

THIS IS the Customer Engineering Manual of Instruction for the IBM 7503 Card Reader and the IBM 7614 Card Reader Control of the 7030 System. The material presented is based on the information available for the commercial 7030 System as of October 17, 1960. Areas of the System are covered as shown in the frontispiece.

The manual contains material on:

1. The IBM 7503 Card Reader as a functional part of the 7030 System.
2. Mechanical operation of moving cards through the reader.
3. Description of the electrical and electronic operations for controlling and reading cards as referenced to the control unit.
4. General Card Reader Control concepts.
5. Internal functions of the Control Unit.
6. Functional operations of the Control and checking circuitry.
7. C. E. Test Panel operation and functions.

This manual, Form R23-9702, obsoletes the Preliminary Instruction Texts on the 7503 Card Reader and on the 7614 Reader Control.



IBM 7030 DATA PROCESSING SYSTEM

CONTENTS

1 IBM 7503 CARD READER

THE IBM 7503 Card Reader (Figure 1-1) provides a means for introducing punched card data into the computer system. The reader contains the electrical and mechanical components necessary to transport, sense, and stack 1,000 standard punched cards each minute. Because the reader contains no logic circuitry or control panel, an intermediate device, 7614 Card Reader Control, is required to unite the card reader with the computer system and to provide controls.

This part of the manual discusses the theory of operation of the 7503 Card Reader. Maintenance information is found in the IBM Customer Engineering Manual of Instruction 88 Collator, Form R25-4503 under the section titled Card Feed.

The card reader has a single feed and stacker with two reading stations. The standard IBM 80-column cards pass through the following:

1. Feed hopper (1,000 card capacity)
2. First read station
3. Second read station
4. Transport
5. Card stacker (2,000 card capacity)

Card levers indicate the progress of cards through the card reader. Five strap-type contacts are used as card levers as follows:

1. Hopper contact -- indicates the presence or absence of cards in the hopper

2. First card lever contact -- indicates the presence or absence of cards at the first read station.

3. Second card lever contact -- indicates the presence or absence of cards at the second read station.

4. Stacker card lever contact -- indicates the presence of cards in the feed rolls.

5. Stacker stop switch -- indicates a full stacker.

The card feed clutch controls card movement to the second read brushes. When a card passes the second read brushes, the continuously running transport mechanism and random type stacker move the card to the hopper and stack it.

The mechanical operation of the card reader is powered by a 1/4 hp, 60 cycle, 15 volt motor that runs at 1,725 rpm. This motor also drives the rotating arm of the magnetic emitter at 1,000 rpm.

FIGURE 1-1. CARD READER

2 MECHANICAL OPERATION

2.1 MECHANICAL DRIVE

A 1/4 hp motor supplies the power to drive the card reader. The mechanical motion of the motor is transferred to the feed knives and first three sets of feed rolls through the card feed clutch. Figure 2.1-1 shows the card feed mechanism. Whenever the drive motor is running, the following units are in operation.

1. Magnetic emitter armature
2. Card feed clutch ratchet
3. First and second read contact rolls
4. Feed rolls in the transport station
5. Random stacker

Figures 2.1-2 and 2.1-3 are the side views of the card reader mechanism.

2.2 DRIVE CLUTCH

The drive clutch controls the movement of a card from the card hopper to the second read brushes. The drive ratchet makes a one-half revolution each machine cycle. A drive dog and drive detent controlled by the action of the drive arm and the intermediate arm engage the ratchet. The dog and detent are spring-loaded and pivot on studs that are part of the drive arm. The leg and detent are controlled by studs that are part of the intermediate arm. The intermediate arm pivots on a sleeve that is the hub of the drive arm.

The clutch operates as follows: Assume the clutch is latched as in Figure 2.2-1. Impulsing the magnet releases the latch and allows the intermediate arm to move in relation to the drive arm. The intermediate arm moves clockwise because of the spring-loaded dog and detent exerting force on the control studs. As the intermediate arm moves, the dog and detent are allowed to engage the ratchet and rotate the mechanism that drives the feed knives and controlled feed rolls.

Unless the clutch magnet is again impulsed, the clutch will disengage when the opposite end of the arms strike the latch. The intermediate arm, moving clockwise in relation to the drive arm, will strike the latch first. The drive arm continues to move and causes the dog and detent to be cammed away from the ratchet by the motion of the pivot studs with respect to the control studs on the intermediate arm. Inertia carries the drive arm forward to strike the latch and the keeper falls behind it to hold the clutch latched. The clutch is timed to latch at 315^{o}.

2.3 PICKER KNIVES

The picker knives move the cards from the hopper into the first feed rolls. Figure 2.3-1 shows the picker knife drive located under the hopper. A complementary cam (card feed cam) is located on the shaft driven by a timing belt under clutch control. Two cam-follower arms clamped to the picker knife shaft follow the card-feed cam surfaces and transmit motion to the picker knife shaft. Two picker knife arms, also clamped to this shaft, move the picker knife blocks 5/8" through an arc, back and forth.

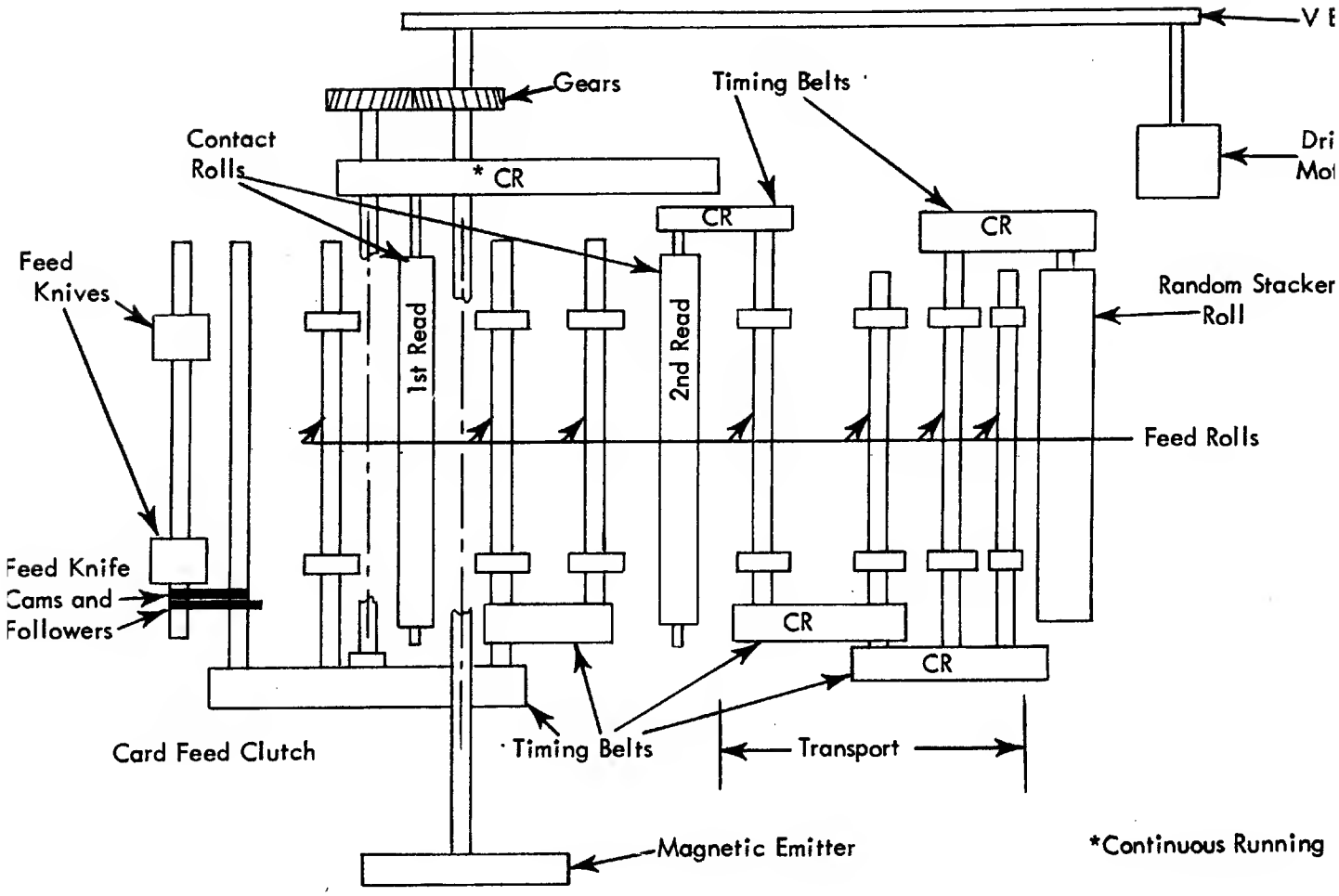


FIGURE 2.1-1. CARD FEED MECHANISM, SIMPLIFIED SCHEMATIC

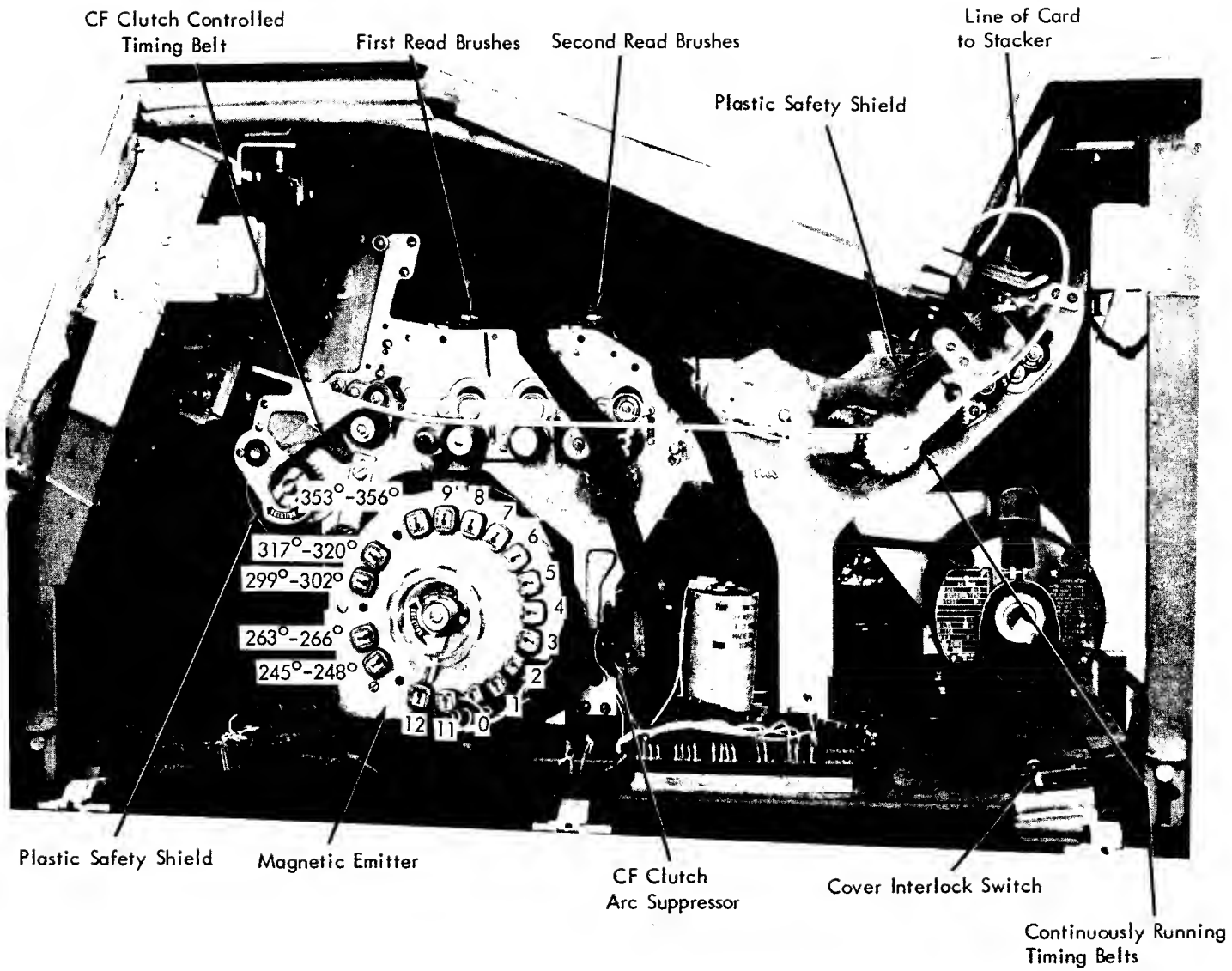


FIGURE 2.1-2. RIGHT SIDE OF CARD READER

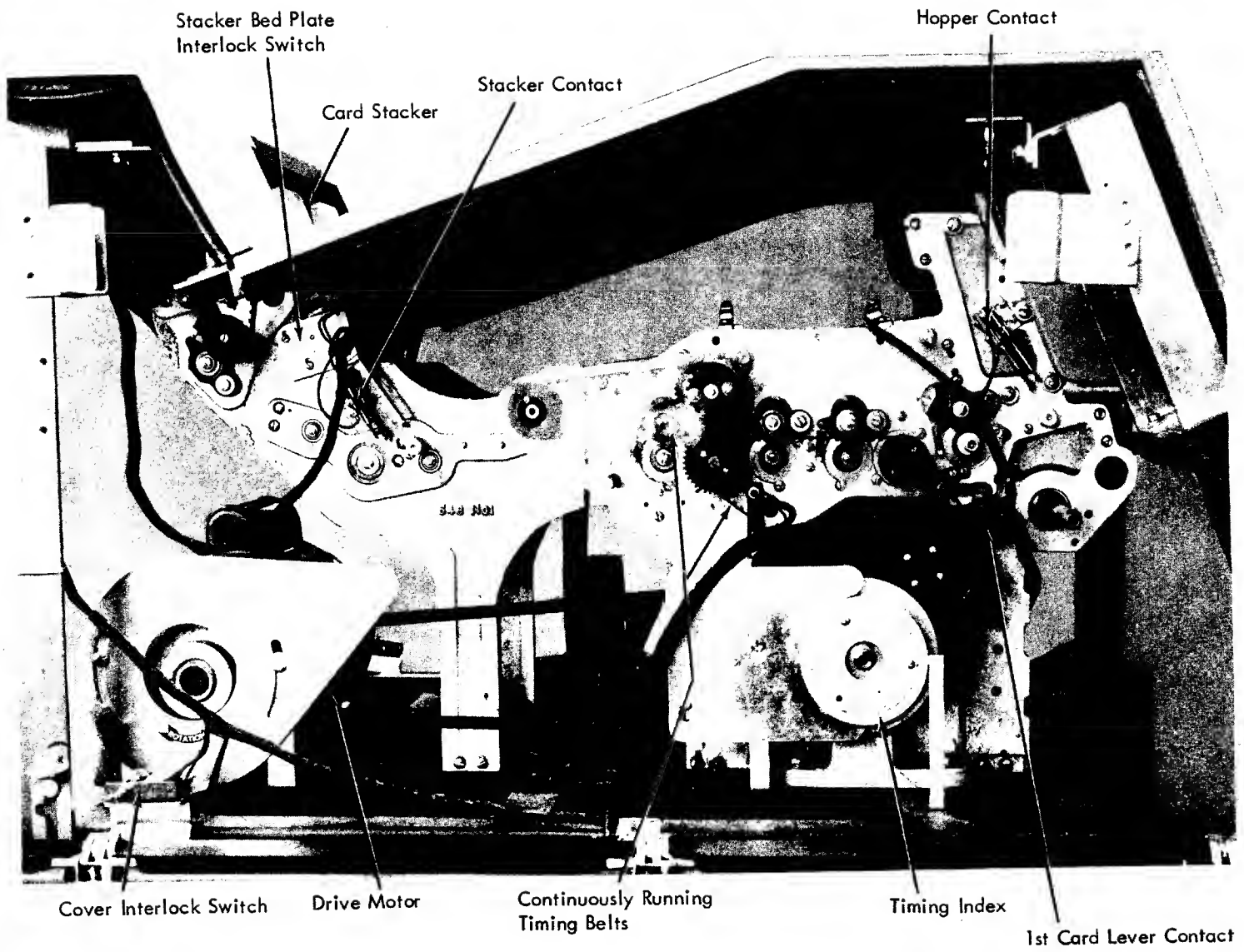


FIGURE 2.1-3. LEFT SIDE OF CARD READER

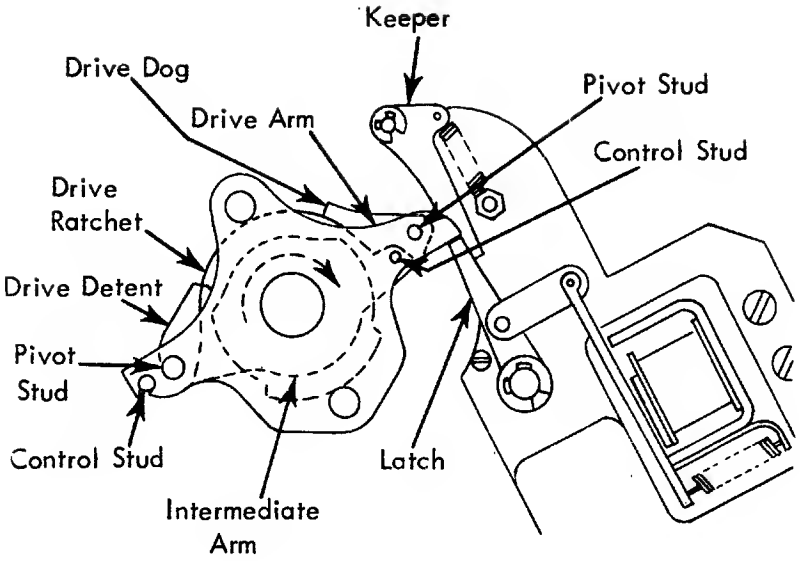


FIGURE 2.2-1. CLUTCH, SIMPLIFIED SCHEMATIC

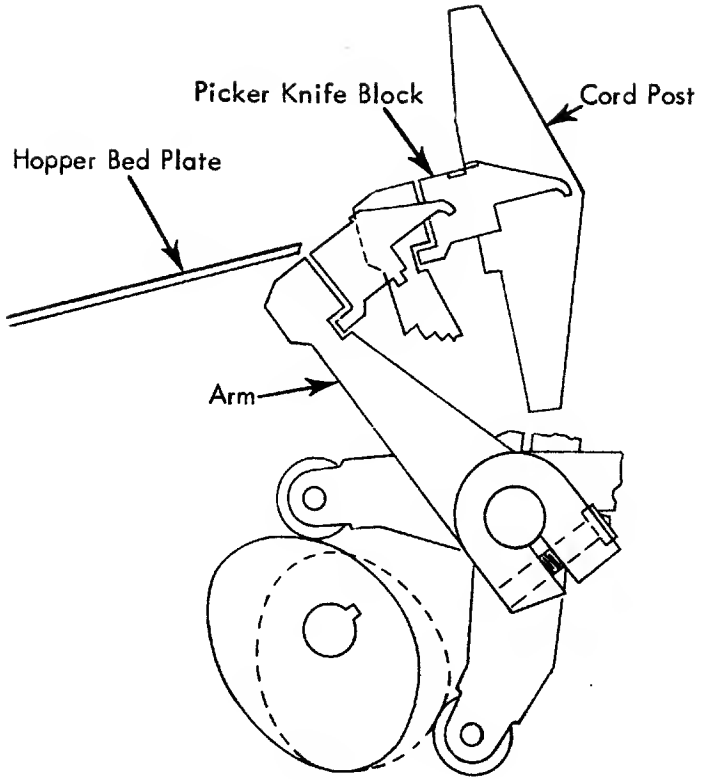


FIGURE 2.3-1. CARD PICKER KNIFE, SIMPLIFIED SCHEMATIC

Because the picker knives travel in an arc and not in a plane parallel to the card, the knife blocks must travel evenly through the same arc to obtain the best possible feeding condition. To define the picker knife arc, consider the center of the picker arm shaft as the center of a circle. The distance from the shaft center to the feeding edge of the knife blocks is comparable to the radius. The card feed cam followers move the knife blocks through an arc of this circle.

2.4 CARD READ STATIONS

Each card read station has 80 brushes and reads the card by rows. The two read stations are used to check that the data are read from each card properly. The first read station is the check reading station; the second read station reads the information for transfer to the computer.

A plastic block containing the 80 read brushes is mounted in a frame. The frame and brush block assembly is fitted into the card reader with guides and locating pins. The brush block is adjustable in the frame for alignment, projection, and timing.

2.5 RANDOM STACKER

The card reader contains a random-type stacker. The stacker bed plate is mounted on top of the reader with the stacker to the rear of the bed. Cards are stacked in the same sequence in which they are read.

The stacker is continuously driven when the drive motor is running. The cards feeding to the stacker need not be timed to the stacker feed roll. A series of card feed rolls moves the card to the rear and up behind the stacker rubber roll. The rubber roll and the card guide feed rolls (Figure 2.5-1) carry the card over and around the rubber feed roll into the stacker bed. The stacker card weight maintains the cards in contact with the stacker rubber roll and insures that the card is moved fully into the stacker.

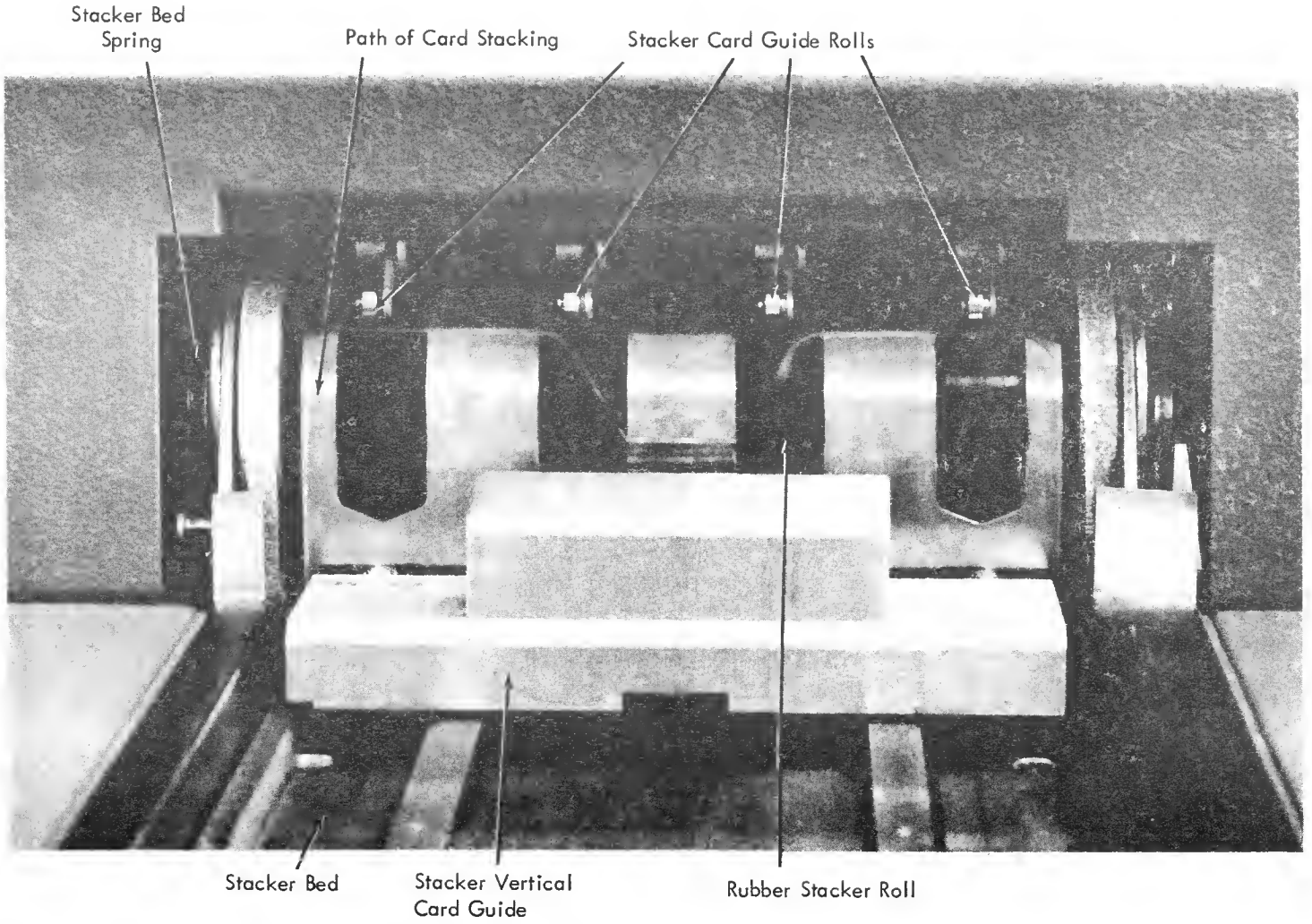


FIGURE 2.5–1. CARD STACKER

3 ELECTRICAL OPERATION

3.1 GENERAL

The card reader contains no logic or control circuits. A -48v power supply provides power to the card levers. The card lever outputs are wired to integrator networks (located in the card reader) that convert the -48v N line levels. The N lines are compatible with the solid state logic circuits in the card reader control unit.

The electrical coils, lights, and read brushes are connected to transistor drivers in the reader control unit. The lines from these units are not wired through integrator networks.

3.2 MAGNETIC EMITTER

The magnetic emitter supplies timed pulses to the card reader. The emitter consists of an alnico permanent magnet that rotates past 17 pickup heads at a rate of one revolution every 60 msec. As the magnet passes each head, the voltage induced in the head is amplified by an amplifier in the head circuit. The amplified pulses are adjusted (by means of variable amplifier bias) to 500 usec duration (3^{o} of head rotation).

Figure 2.1-2 shows the head positions on the circumference of the emitter plate. From 11^{o} to 212^{o}, the twelve heads provide the pulses in synchronism with the card cycle points during card reading. The remaining five heads provide control pulses to the reader control unit.

3.3 TIMER

The timer is located in the card reader and controls the drive motor. The timer consists of a 60 cycle, single phase, 115 volt timer motor, an adjustable timing mechanism, and a cam-operated contact. The timing mechanism is set for a specific time interval. When the timer motor runs for this interval of time, a can actuates the timer contact to close it. The output of this timer contact, fed through an integrator, resets the drive motor control circuit in the reader control unit. Hence, when the timer contact is made, the card reader drive motor is stopped. This timing device permits the drive motor to be stopped if the computer does not request card reader use for a preset time interval. Because the read station contact rolls are continuously running, the drive motor is stopped to prevent contact roll wear.

3.4 LIGHTS, KEYS, AND SWITCHES

The lights, keys, and switches are mounted at the upper right front of the card reader (Figure 3.4-1) and, with the exception of the power-on light, are controlled by the reader control unit. This external unit is the intermediate unit between the card reader and the data processing system.

FIGURE 3.4-1. CARD READER SWITCHES, KEYS, AND LIGHTS

3.4.1 Switches and Keys

Master Switch -- controls the external application of all power to the machine; must be on before power can be applied.

Power-On Switch -- turns on all AC and DC power except 60 cycle, phase 1. This phase is under control of the master switch and is on as long as the master switch is on.

Power-Off Switch -- turns off all power except 60 cycle, phase 1 which is available at the convenience outlets behind the front cover of the electrical component assembly.

Motor Switch -- controls the AC to the drive motor. This switch must be on to operate the machine.

Start Key -- depression of this key will start feeding cards if cards are in the hopper and are not in the reading stations. The machine should take three card cycles, leaving the first card in the stacker, the second card in the second read station, and the third card in the first read station. Depression of the start key turns on the ready light if the machine had been stopped in a normal card cycle.

Stop Key -- depression of this key stops the feed and the drive motor at the end of the present card cycle. It also drops the machine out of the ready status and turns off the ready light.

Unload Key -- depression of this key causes the feed to run as long as the key is depressed, provided the machine is not in ready status and there are no cards in the hopper.

Signal Key -- depression of this key sends a signal for computer use.

3.4.2 Indicating Lights

Power-On -- on as long as DC voltages are present in the card reader.

Ready -- turned on by (a) taking a run-in cycle or (b) depressing the start key after the card reader has been stopped with the stop key during normal running. Malfunctions in feeding and the interlock circuits will turn the ready light off.

Out of Material -- turned on whenever the stacker switch is operated when the hopper is empty of cards or the last card has passed the second read station. The next depression of the start key turns off this light.

Feed Check -- turned on by any malfunction in the normal feeding of cards. The next depression of the start key turns off this light.

Read Check -- turned on by computer control to indicate that a read error has been detected. The next depression of the start key turns off this light.

Reserve -- turned on or off by computer instruction.

3.5 SAFETY INTERLOCKS

The card reader has interlocks that monitor the three side covers and the stacker bed plate. The interlock contacts are shown in Systems 10.00.02.1. If one or more of the interlocks are open, the DC voltage is removed from all brushes, card lever contacts, and lights (except the power-on light). This power-on light remains on to indicate that the DC voltage power supply is still up. The four interlocks and their interlocking conditions are:

Stacker -- opens if the stacker tray is not in position to receive read cards.

Right Cover -- opens if the right side cover is not completely closed.

Left Cover -- opens if the left side cover is not completely closed.

Rear Cover -- opens if the rear side cover is not completely closed.

The three cover interlocks can be closed manually when the covers are open to facilitate maintenance. The cover interlocks are reset when the covers are closed.

3.6 COMPONENT LOCATION

Connectors, circuit breaker, convenience outlets, the timer, and integrators are mounted on the front of the lower inner front panel of the card reader (Figure 3.6-1). Terminal boards 1 and 2, and heavy duty relays 1, 2 and 3 are mounted on the rear of this same panel. The connectors on the front of the mounting panel are SC1-SCS and PP1 and PP2. The following table indicates the association of these connectors to the IBM 7614 Card Reader Control unit connectors:

Card Reader Connector	Assignment	Reader Control Unit Connector
SC1	First read brush wires 1-40	D5
SC2	First read brush wires 41-80	C5
SC3	Second read brush wires 1-40	B5
SC4	Second read brush wires 41-80	A5
SC5	DC ground lines -48v line	D4
SC6	Magnet emitter lines	B1
SC7	Integrators and card reader lights	C1
SC8	Control lines	D1
PP1 (26 Positions)	60 cycle power lines	F (26 Positions)
PP2 (8 Positions	400 cycle power lines	D (8 Positions)

The circuits in the card reader are found on Systems 10.00.01.1 through 10.00.04.1.

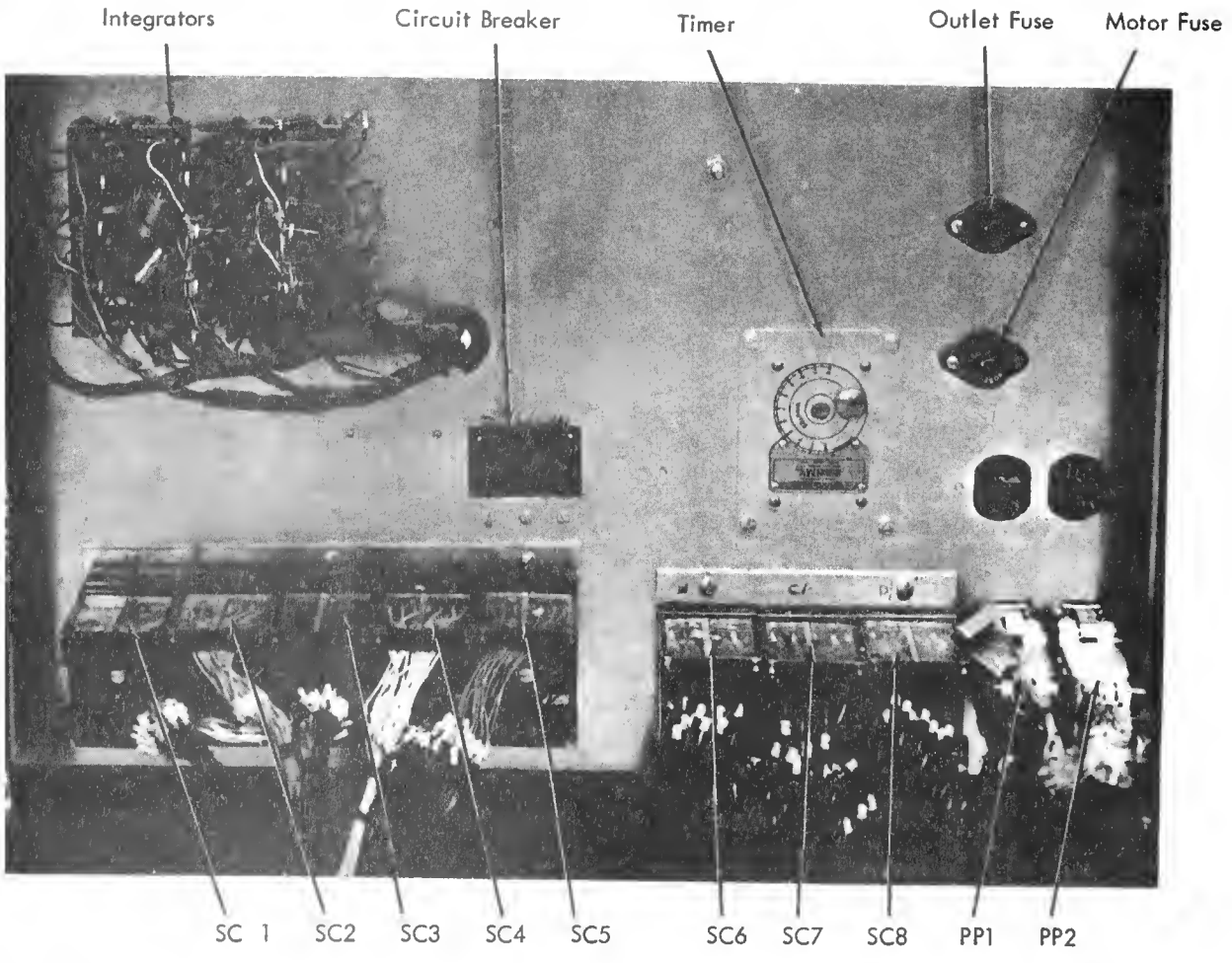


FIGURE 3.6-1. COMPONENT LOCATION, LOWER FRONT MOUNTING PLATE

4 IBM 7614 CARD READER CONTROL

4.1 INTRODUCTION

The IBM 7614 Reader Control provides the circuitry to read punched card data into the IBM 7030 Data Processing System. The punched card is read at the IBM 7503 Card Reader (1000 CPM) and the data are stored in core storage buffers in the reader control unit. Upon request from the IBM 7619 Exchange, these data are sent to the exchange and transferred to the core storage units of the 7030 System. Neither the reader control unit nor the card reader have control panels. These units are controlled by the exchange which monitors the functions and operation of the I-O device. The reader control unit has data and functional check circuits.

The reader control unit controls the card reader, stores data in ferrite core buffers, and transmits data to the exchange. Data bits are transmitted in groups of eight over eight parallel lines. One group of eight data bits is referred to as a byte of data. In addition, a ninth line, also parallel to the data bit lines, transmits a parity bit for data-checking purposes at the exchange. A block of data (the data in one punched card) is transferred to the exchange in 120 eight-bit bytes with an associated parity bit for each data byte.

4.2 GENERAL DATA FLOW (Figure 4.2-1)

The IBM 7614 Card Reader Control accepts and stores data read from punched cards at the IBM 7503 Card Reader. Each of two read stations in the card reader supplies card data to the reader control unit. The data from the first read station enter either of two check buffers in the reader control. The data from the second read station enter the record buffer. These three buffers in the reader control have a full data card capacity: 960 bits. During the initial card loading and run-in at the card reader, the data buffers are loaded in the reader control and the reader control is made ready to accept programmed instructions.

The reader control and the card reader are controlled from the main program (these units do not contain control panels). When a programmed read instruction is encountered, a read signal is directed to the reader control through the IBM 7619 Exchange. If the reader control is in a ready status, the read signal initiates a read operation.

The read operation transfers the data stored in the record buffer to the exchange. Data are transferred by a sequence of data bytes (eight data bits and a parity bit) and 120 bytes are required to empty the record buffer. When the last data byte is transferred to the exchange, an end-of-message is signalled to the exchange and the card feed clutch is energized in the card reader. The end-of-message will disconnect the reader control from the exchange; if a subsequent read operation is programmed, another read signal restarts the next read operation. The card feed clutch feeds a card past each read brush station in the card reader to reload the buffers. Another read operation cannot start until this card feed cycle (that is, card reading) is completed.

The card reader control and card reader operate in either of two modes. These modes (non-ECC mode and ECC mode) are performed in the same basic manner. The difference

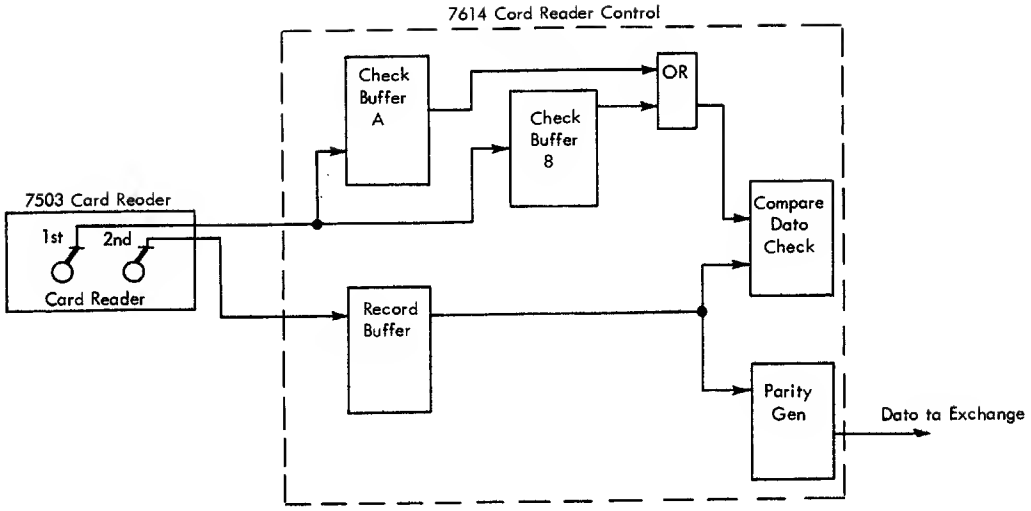


FIGURE 4.2-1. DATA FLOW - READER CONTROL

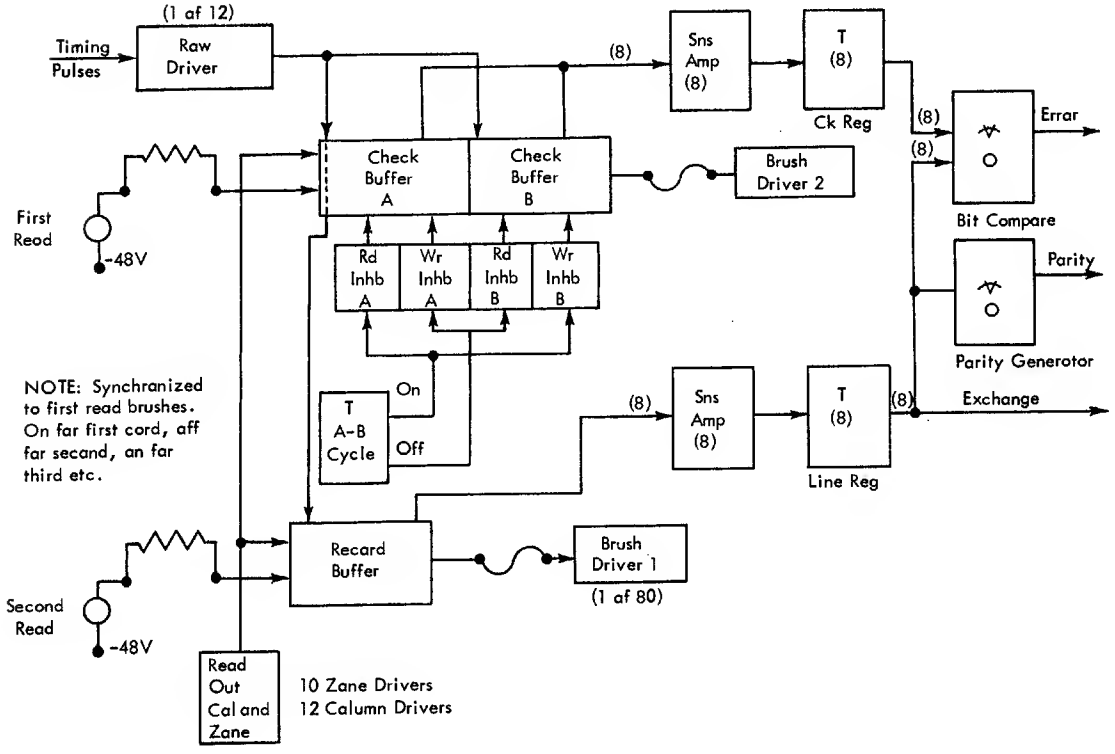


FIGURE 4.2-2. CARD READER DATA FLOW

between these modes is the length of the data word transferred to the exchange from the card.

The internal machine data word is 72 bits long, containing eight ECC bits plus 64 data bits. The 64 data bits constitute either program instructions or operational data. The eight ECC bits assigned to each word provide a means of checking the data bits as these data are manipulated. If a single error is detected in any bit of the data word, the error is automatically corrected; or, if any ECC bit is in error, it also is corrected. A double error in the data bits is detected but cannot be corrected. Hence, the 72 bit data word is self-correcting when a single error occurs.

The cards read in the card reader may be punched with either 72-bit data words (ECC mode) or 64-bit data words (non-ECC mode). The reader control and card reader can be programmed to read cards punched in ECC mode. Normally, these units are in non-ECC mode. Because eight bit bytes are transferred serially, eight such bytes transfer a data word in non-ECC mode, and nine bytes transfer a data word in ECC mode.

Data normally is transferred from the card reader control unit to the exchange during a read operation. However, when a control instruction is programmed to the card reader channel, data (one eight-bit byte) are transferred from the exchange to the card reader control. This instruction gives the program the ability to perform a function at the card reader control. (Altering the card reader control to the ECC mode of operation is a control function.) One eight-bit byte of data (the control function code) must transfer from the exchange to the reader control, where it is decoded to the function desired.

The read operation consists of transferring data (loaded in the record buffer in the reader control) to the exchange. When the buffer is emptied, a card feed cycle is started in the card reader to reload the record buffer.

With data transfer, card reading is checked. The card data read at the first brushes are entered into a check buffer. When this same card is read at the second read brushes, the data are stored into the record buffer. As the data transfer to the exchange is initiated, both the check buffer and the record buffer are read out simultaneously. These data are compared to verify that the card has been properly read.

Figure 4.2-2 is a more detailed flow diagram of Figure 4.2-1. In Figure 4.2-2 the read-in and read-out drivers and the output registers are shown. These units are explained in subsequent sections of the manual.

4.3 MACHINE LANGUAGE (Figure 4.3-1)

The data punched in the IBM card used with the 7030 System is in a binary form. Each card punch position is a possible data bit, with a punched hole representing the data bit. The card is capable of storing 960 bits (80 x 12).

The relationship of the data bits punched on the card to the data bits assembled into machine data words is shown in Figure 4.3-1. Although the card is read in rows (starting from the 9 row through the 12 row), the data are transmitted in column to the exchange. Figure 4.3-1 shows the first six-card columns with the 72 data bit positions enumerated. The larger number represents the byte in which the data bit is sent to the exchange, and the small number represents the data bit position within each byte.

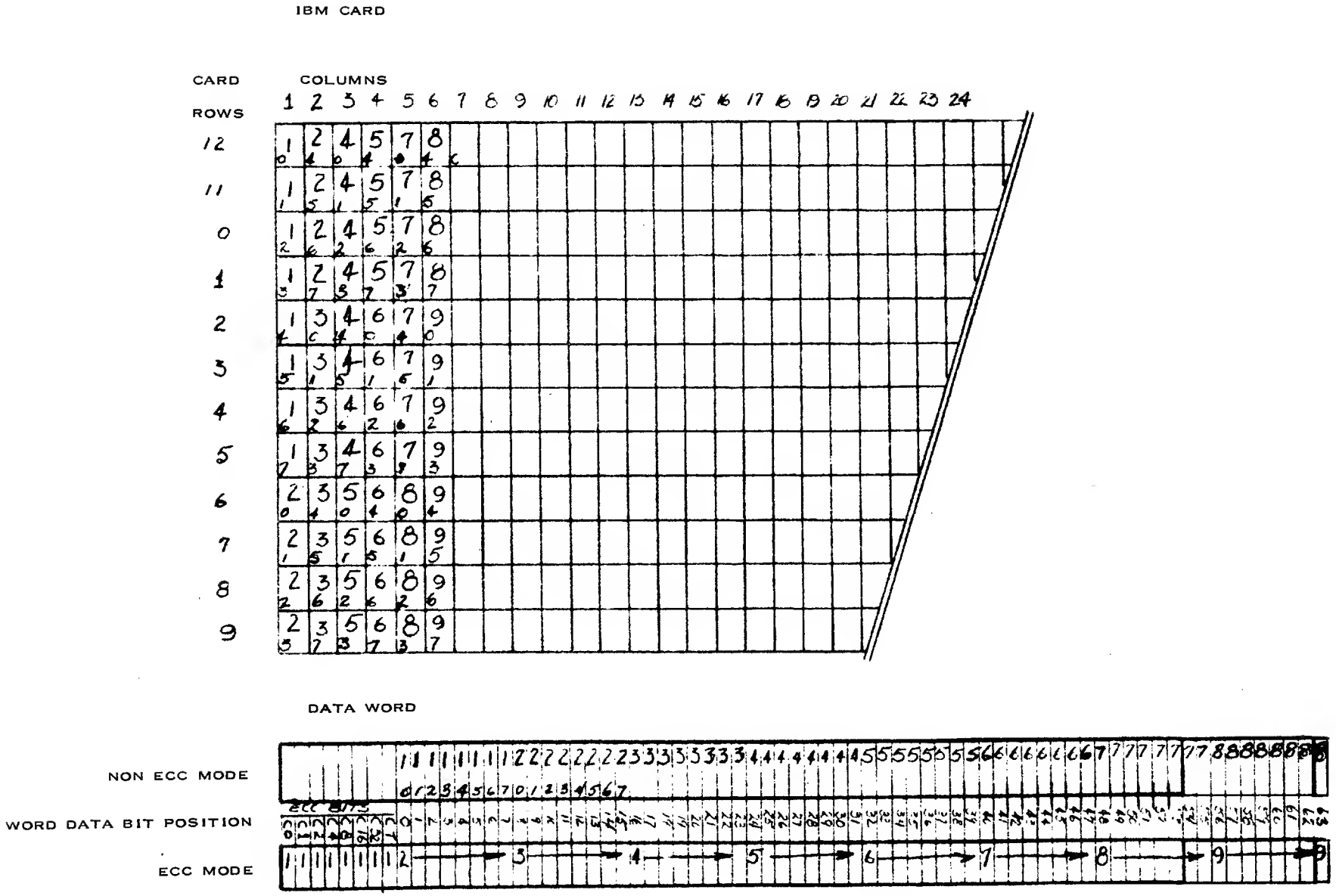


FIGURE 4.3-1. DATA BIT RELATION-CARD TO DATA WORD

As the data are received by the exchange, they are assembled into 64 or 72 data bit words. The bit length of these data words is determined by the format in which the data card is punched. If the data card is punched in a 64-bit word format, the data words are assembled in the exchange as 64-bit words. Similarly, a 72-bit word in the card is assembled as a 72-bit word in the exchange. Regardless of the length of the assembled word at the exchange, the data word sent to main core storage is always 72 bits long.

Data words in the IBM 7302 Core Storage Unit of the 7030 System are 72 data bits long. These words contain 64 data bits and eight error checking and correcting (ECC) bits. The eight ECC bits are used to check the positions of a word fetched from core storage by any unit of the system. When the card is punched in a 64-bit format, the exchange generates eight ECC bits that are affixed to the 64 bits of data and transmits the 72-bit word to core storage.

Cards punched in a 64-bit word format are assembled in a non-ECC mode as shown in Figure 4.3-1. The first byte sent to the exchange consists of the first eight data bit positions of card column 1. The second byte consists of the last four bit positions of card column 1 and the first four of card column 2. The third byte consists of the last eight bit positions of card column 2. Figure 4.3-1 illustrates the card location of the 4th, 5th, 7th, 8th and 9th bytes and the bit position of any bit within a byte.

In a non-ECC mode, the exchange will assemble a 64-bit word and the bit and byte locations within the data word are shown in Figure 4.3-1. In a non-ECC mode, the first 5 1/3 card columns, 64 consecutive bits, define a data word. The card has a capacity of 15 data words in this mode. Cards punched with 72 bit data words are in an ECC mode, and six card columns define a data word. In this mode, the first byte of each data word in the card contains the ECC bits. A card in ECC mode has a word capacity of 13 data words. The last two columns of the card (79 and 80) are not transmitted to the exchange. Nine bytes are assembled at the exchange into a 72-bit word. The relative position of the card data to the assembled data word in the exchange is shown in Figure 4.3-1.

4.4 PHYSICAL LAYOUT

The reader control unit is packaged in an SMS swinging gate cube (Figures 4.4-1 and 4.4-2). Six swinging gates of logic contain the solid state circuits. The A module of the cube contains four gates of circuitry, a 300w modular power supply, and the Customer Engineer test panel. The CE test panel occupies the area normally assigned to gates A1 and A2. The four gates of circuitry are located in gate positions A3, A4, A5 and A6. The power supply is mounted in gate position A8. The area of gate A7 is empty.

The B module contains two gates of circuitry, the core array, the cable connectors, circuit breakers, and the read brush winding resistors. The brush winding resistors are assigned to gate area B1. The cable connectors and circuit breakers are mounted in the B8 gate area. The two gates of circuitry are hung in locations B5 and B6. The core array is located in B4. Gate positions B2, B3, and B7 are not used.

4.4.1 Terminal Boards (TB)

The terminal board locations in the reader control unit are:

TB-1 is mounted above the Burndy 8 and 26 position connectors and behind the connector mounting plate in gate location B8.

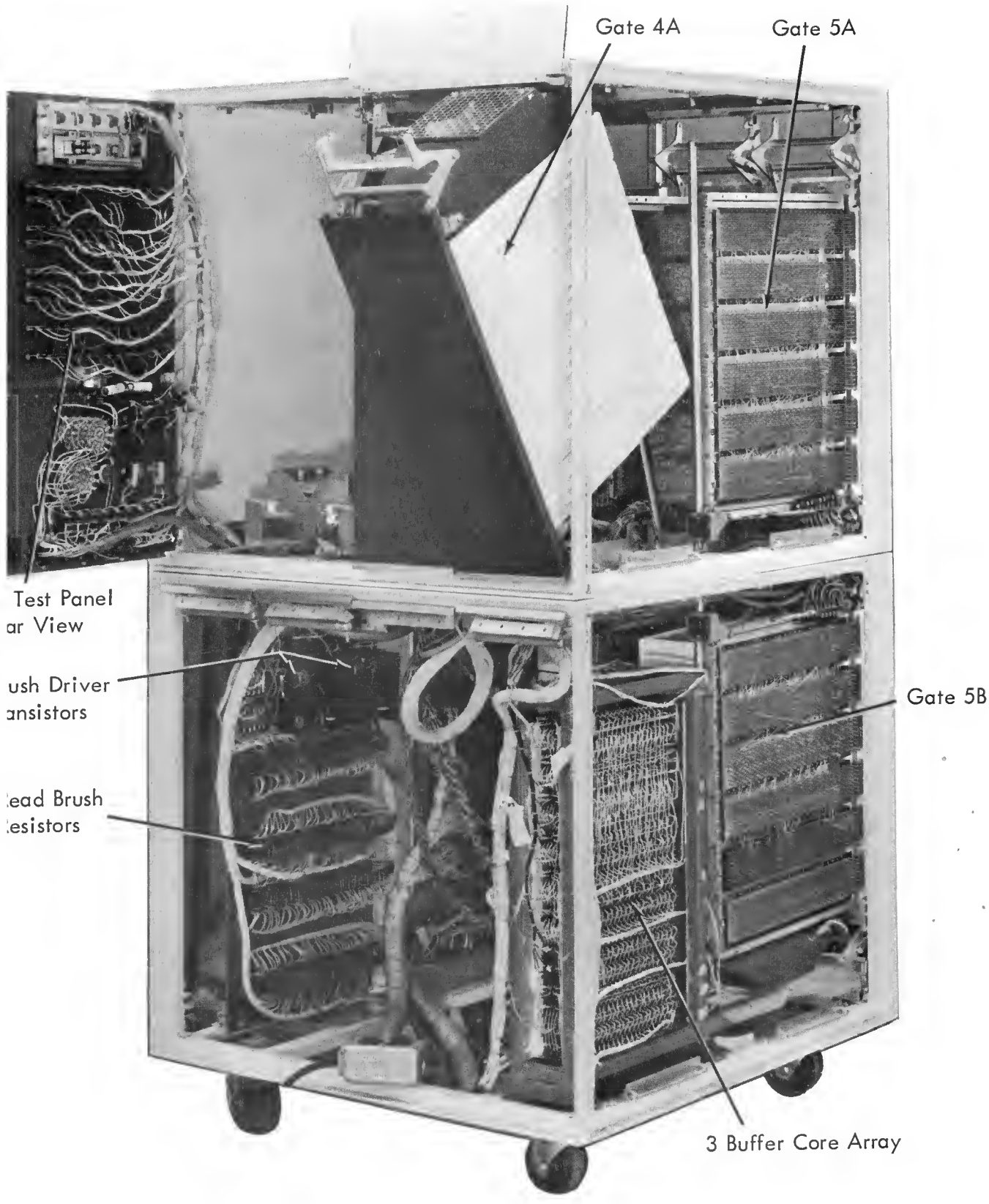


FIGURE 4.4-1. READER CONTROL IN ASSEMBLY (FRONT VIEW)

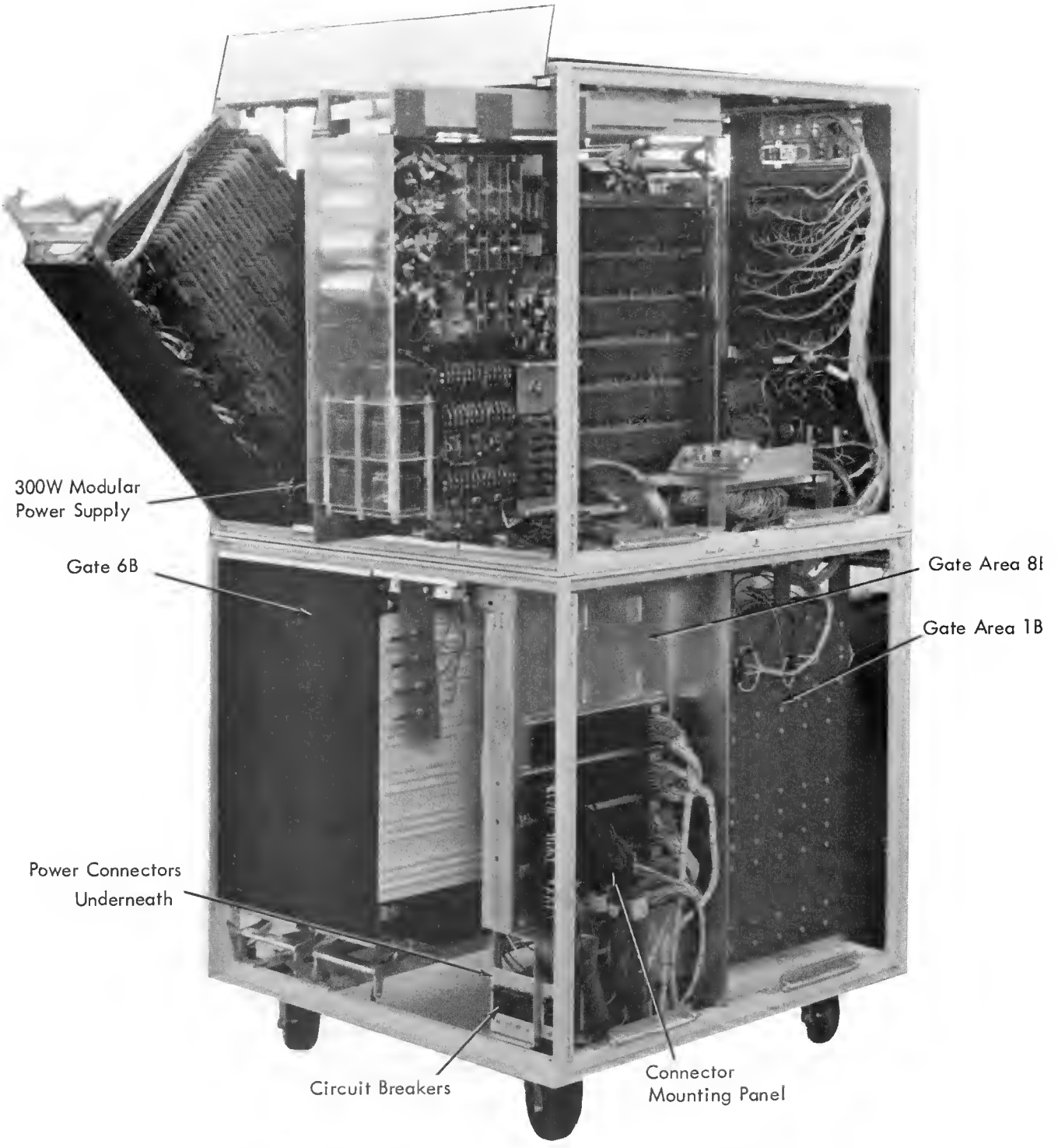


FIGURE 4.4-2. READER CONTROL IN ASSEMBLY (REAR VIEW)

TB-2 is mounted on the rear side of the connector mounting plate in location B8.

TB-4 and 5 are mounted on the front horizontal cube frame member near gate area A2 and A3.

TB-6 and 7 are mounted on the rear horizontal cube frame member near gate area A6 and A7.

Terminal boards 5, 6, 7 distribute the DC supplies to gates A3, A4, A5, A6, B5, and B6.

4.4.2 Cable Connectors

The cables that tie the reader control unit to the card reader, the exchange, and the power distribution frame (PDF) enter the reader control unit at gate location B8. Ten 40-position Burndy cable connectors are mounted vertically on the connector mounting plate at location B8. The following is a list of the 40-position connectors and their assignment:

Connector Number	Cable Assignment
A5	Second read brush wires 41-80 from the card reader.
B1	Magnetic emitter timer pulses from the card reader.
B5	Second read brush wires 1-40 from the card reader.
C1	1. Lines from the card reader contacts and switches. 2. Lines to the card reader indicator lights and timer bias.
C2	1. Output lines to the exchange. 2. -36v line from the exchange.
C5	First read brush wires 41-80 from the card reader.
D1	Control lines to the card reader.
D2	Input lines from the basic exchange.
D4	DC ground lines from card reader
D5	First read brush wires 1-40 from the card reader.

Four additional Burndy connectors are mounted horizontally on the connector mounting plate. Two connectors are 8-position and two are 26-position Burndy units. These connectors tie the 60 cycle and 400 cycle power lines between the reader control unit, card reader, and the power distribution frame. The connectors are designated C, D, E, and F. The C and D connectors tie the 400 cycle lines; E and F connectors tie the 60 cycle lines. The association is:

Connector	
C (8 pos)	400 cycle lines to the power distribution frame.
D (8 pos)	400 cycle lines to the card reader.
E (26 pos)	60 cycle lines to the power distribution frame.
F (26 pos)	60 cycle lines to the card reader.

The connector used and the pin location of the communication lines are shown on Systems 00.02.01.0 through 00.02.06.0 The pin locations of the core array are shown on Systems 00.12.01.0 through 00.12.08.0.

4.5 COMMUNICATION LINES (Figure 4.5-1)

The reader control unit is connected to the exchange by one of 32 possible exchange channels. In addition, the control unit is connected to the card reader with control and signal lines. Figure 4.5-1 shows these lines and their directions from the reader control unit.

4.5.1 Exchange to Card Reader Control

Write: Eight write lines are used to send information to the reader control during a control operation. This operation is initiated by the main program when a control instruction is encountered in the program. These lines feed an eight-bit byte to the line register.

Write Parity: Permits a parity bit to accompany the eight bits transmitted to the reader control unit during a control operation. This parity bit enters the line register with the control operation information and is generated for odd parity data checking.

Byte Response: Used to inform the reader control that the exchange has recognized and honored a service request sent by the reader control unit. This line, during a read operation, indicates that a byte of data has been accepted by the exchange and the successive byte may be transmitted.

Read Instruction: Initiates a read operation if the card reader is in a ready status and is not busy.

Write Instruction: Sends a write instruction signal to the reader control. However, a write instruction cannot be performed by the reader, and an exchange program check and an end-of-message are signalled to the exchange.

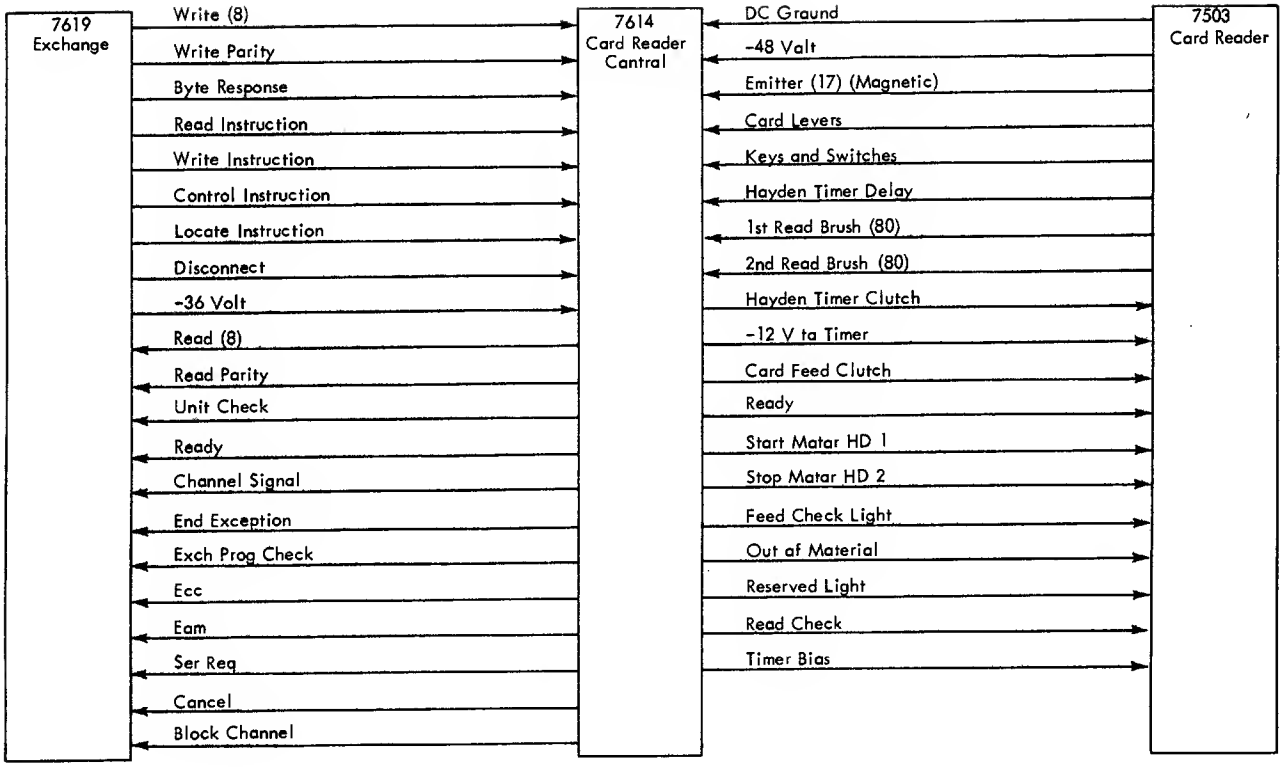


FIGURE 4.5-1. COMMUNICATION LINES

Control Instruction: Starts a control operation to perform some desired function at the card reader.

Locate Instruction: Sends a locate signal to reader control. However, the locate operation cannot be performed by the reader control unit, and an exchange program check and an end-of-message are signalled to the exchange.

Disconnect: Is initiated at the exchange when the end-of-message (EOM) trigger is turned on at the reader control. The disconnect line resets triggers in the reader control to divorce the card reader from the exchange control. The disconnect line may be activated from the exchange before the EOM trigger is turned on in the reader control. In this case, the signal is defined as an early disconnect. This early disconnect blocks further data transfer from the reader control to the exchange. The reader control continues to read out the remaining data from the record buffer and a card feed cycle is initiated at the card reader. The card feed cycle reloads the data buffers in the reader control for the next read operation.

-36 Volts: Supplies -36v to the D level of the rotary deck switch on the CE test panel.

4.5.2 Reader Control to Exchange

Read: Eight lines transmit the data bytes to the exchange during a read operation. Eight data bits are sent in parallel as a byte of data.

Read Parity: Carries the parity bit sent with each data byte. The parity bit permits data transmission checking when the data reach the reader control. Odd-parity checking is employed by all I-O devices for data transmission.

Unit Check: Is the output of the unit check trigger in the reader control. It indicates that an uncorrectable data error has occurred in the current read operation. The Unit check status bit is set in the control word in the exchange at the end of the current block of data.

Ready: Signifies that the card reader is loaded with cards and is in a status to accept a read or control instruction from the main program.

Channel Signal: Is active when the reader is initially placed in a ready status or when the signal key is depressed at the card reader. A channel signal status bit is set in the control word in the exchange. This status bit may be interrogated by the program as a decision element.

End Exception: Is active when the card reader stacker is full or when the reader runs out of cards. The out-of-material light is illuminated at the card reader by an end exception condition. When the reader runs out of cards, the end exception indication is not given until the data of the last card have been transmitted to the exchange. If the current read instruction requires additional data, more cards must be loaded and run in the reader. An end exception status bit is set into the control word. This status bit permits the system to recognize that the card read is in an out-of-material situation.

Exchange Program: Is activated when a write or locate instruction is programmed to the card reader, or when the control code during a control operation is invalid. An exchange program check status bit is set in the control word in the exchange.

Error Checking and Correcting (ECC): Is active when the reader control is in ECC mode. Whenever data cards that are punched in an ECC mode are to be read by the card

reader, the reader control is first placed into ECC mode. A control instruction, which specifies ECC mode, must precede the read instruction in which ECC punched cards are read.

End of Message: Indicates that the current operation (read or control) is terminated and that the reader control is to be disconnected from the exchange channel. Any unusual condition which turns on the cancel trigger in the reader control will also initiate the end-of-message. The exchange responds with a disconnect signal to reset various triggers in the reader control.

Service Request: Indicates to the exchange that a byte of data is on line ready to be accepted during a data transfer (read) operation. During a control operation, this line signifies that the reader control is ready to accept control information. When the exchange accepts a byte of data during a read operation, it transmits a byte response to the reader control.

Cancel: Indicates that an unusual condition is recognized at the card reader or control unit such as card feed failure or circuit failure.

Block Channel: Carries a -36v back to the exchange to block the channel to which the reader control is connected while the CE test panel is in use.

4.5.3 Card Reader to Reader Control

DC Ground: These lines are connected to the brush driver transistor circuits in the reader control.

-48 Volts: Supply the collector circuit of the brush driver transistors.

Magnetic Emitter (17): From each of the magnetic emitter pick-up heads; supply the magnetic emitter pulses to the reader control during a card feed cycle.

Card Lever: Permit the reader control unit to sense the condition of the hopper contact, card lever 1, card lever 2, and the stacker contact.

Keys and Switches: Are activated by the following keys and switches at the card reader: stacker switch, unload key, start key, stop key, signal key, motor switch off or on.

Timer Delay: Is activated to turn off the card reader drive motor. If a read instruction is not received for a predetermined time interval, the line resets the drive trigger in the control unit.

The First and Second Read Brush: 80 first-read and 80 second-read supply the read buffer with core write current during a card feed cycle.

4.5.4 Reader Control to Card Reader

Time Clutch: Energizes the Haydon timer clutch if a read operation is not in progress at the reader control.

Time Clutch -12v: Is a return line to a resistive load for the timer clutch line.

Card Feed Clutch: Energizes the card feed clutch at the card reader.

Ready Light: Illuminates the ready light at the card reader switch panel when the unit is ready.

Start Motor HD 1: Energizes the heavy duty 1 relay to complete the motor start circuit in the card reader.

Stop Motor HD 2: Energizes the heavy duty 2 relay to open the motor run and complete the motor stop circuit. The stop circuit dynamically stops the motor .

Panel Lights: Illuminate the following lights when activated: feed check light, out-of-material light, reserve light, read check light.

Timer Bias: Provides a bias to the magnetic timer pick-up heads in the card reader. The line voltage is regulated at the reader control to obtain a definite signal level from the magnetic emitter pick-up heads.

4.6 PROGRAM CONTROL

The card reader cannot execute a write or a locate instruction. If either of these units are controlled from the main program of the system. Operator intervention is, therefore, maintained at a minimum. The operator is required to load and run-in the cards at the card reader and to investigate any unusual conditions (feed check, write check) that may occur.

The reader control receives functional signals from the 7619 exchange to start an operation at the card reader. During the operation, the control unit checks and controls the card reader. Any unusual card reader conditions detected by the check circuits of the reader control are signalled to the exchange where these conditions are stored in a register in the computer. The 7030 system has the ability to analyze these unusual conditions. The programmer can, therefore, take advantage of this error analysis of the computer and program sub-routines for the different condition that may occur at the card reader or reader control.

The card reader cannot execute a write or a locate instruction. If either of these instructions are programmed to the card reader, a program check error will result. The write instruction is invalid, for obvious reasons. The locate instruction, however, is invalid to the card reader because only one card reader is assigned to each reader control unit. The locate instruction is used to specify one particular I-O device where more than one I-O device is serviced by one control unit. Five basic instructions are applicable to the I-O devices. These are: RD, WR, LOC, CTL, and REL.

4.7 CHECKING CIRCUITS

Inherent checking features of various functional circuits and components, within the reader control, monitor the card reader and data transmission. Five check circuits survey the machine operation in the following areas:

Unit Check -- ensures the validity of the data entering or leaving the reader control unit. During a control instruction operation, the control code received by the reader control unit is parity-checked. Similarly, during a read operation the transmitted data

are checked in a compare circuit. When a parity error or a compare error is detected (in their respective operations), the unit check indication is given by the reader control.

During an ECC mode read operation, the unit check is turned on if two bit errors are detected within one word (72 bits). In the ECC mode read operation, single read errors within any one word are correctable by the ECC bits associated with the word.

The unit check indication does not interrupt data transmission; but the current operation is terminated at the end of the current block of data. When the operation terminates, the unit check indication and the end-of-operation indication are set in the card reader control word in the exchange.

Driver Check -- provides an operational check of the core buffer read-in and read-out drivers. The row core drivers, the column core drivers, the zone core drivers, and the pulse power supply are checked by the driver check circuit. The combination of the twelve row drivers and the pulse power supply set check cones during buffer read-in, and the column and zone drivers read out these cones. If (during a read-out operation) a check cone is not sensed, the driver check is indicated.

Ring Check -- verifies that the carry operation and the byte counter coincide at the 120th byte. As the reader control transmits data to the exchange, a byte counter counts each byte emitted. When the buffer read-out drivers (column drivers and zone drivers) are advanced to the 120th byte position (carry signal), the byte counter must also indicate a value of 120. An error is indicated if the byte counter is less than 120 when the carry signal is generated.

Feed Check -- made during a card feed cycle. This check examines the card levers during the feed cycle to ensure satisfactory card operation. Either driver check, ring check, or feed check initiate a cancel operation. Should an error condition be detected by these checks, the cancel signal turns on the end-of-message (EOM) trigger. The exchange responds with a disconnect signal to terminate the operation immediately.

Program Check -- monitors the program instructions directed to the card reader. Should a write or locate instruction be addressed to a card reader exchange channel, the program check latch is turned on to indicate the program error. Similarly, when a control operation is in progress at the card reader, the function codes are examined for a valid bit structure. An invalid control function code turns on the program check latch.

When the program check latch is turned on, a signal is supplied to the exchange. This signal sets the Exchange Program Check (EPGK) indicator at the exchange, and the card reader operation is never started. The EPGK check indicator has the highest interrupt priority of the I-O check indicators.

5 INTERNAL FUNCTIONS

5.1 THEORY OF CORE OPERATION

The magnetic core theory is explained in the IBM Customer Engineering Manual of Instruction 7302 Core Storage Manual, Form 223-6838.

5.1.1 Core Buffer Array (Figure 5.1-1 and 5.1-2)

The reader control unit contains a core storage array to accept and store the data read from the punched cards. This array consists of three buffers (check buffer A and B, and record buffer), each of which has the capacity to store 960 bits or one card image. The buffers are further divided into six core planes and each core plane consists of five rows of cores with 40 cores per row. Four core rows in these planes are utilized to store 160 bits of card data. The fifth row of cores is used in the check buffers A and B only (12 planes). These fifth rows in the twelve core planes are used to check one of the twelve row drivers and the column and zone drivers during a read-out operation. The fifth row of cores in the record buffer is not used.

The core array physically is arranged into a vertical stack of 18 core planes. The topmost six planes compose check buffer A, the next six planes (planes 7-12) make up check buffer B, and planes 13 to 18 incorporate the record buffer. Systems 00.12.03.0 through 00.12.09.0 provide pin charts and specific wiring information for the core storage array.

5.1.2 Principles of Core Buffer Read-In (Figure 5.1-3)

The buffer cores read-in current is supplied by the row drivers and the card column brushes. The row-driver windings, from row 9 through row 12, supply half-write current to 80 cores at each card cycle point. Each brush winding supplies half-write current to twelve cores when a punched hole is sensed. The coincidence of the row driver and a punch in the card, sensed by the read brush, provides the necessary write current to set one core. The row drivers supply 275 milliamperes of current for half-write current, but the brush driver need supply only one fourth of this amount, because the brush winding is threaded through its corresponding cores four times. The required half-write current supplied by the brush is the sum of the four brush windings through each core.

Figure 5.1-2 shows the relation of the row driver windings and brush windings to the six planes that constitute a buffer. The brush windings are divided into an odd and an even group, and each group is wired through three core planes. Therefore, each brush supplies one half write current to twelve cores simultaneously. Each row driver is wired through two planes per buffer, and four row drivers are assigned to each pair of planes. The row drivers are wired through a corresponding row of cores in each plane. This allows each row driver to supply half-write current to 80 cores when the driver conducts.

The card travels through the card reader, 9 edge forward, face down. The 80 read brushes sense the card as it moves through the read station and the twelve row drivers conduct, successively, in synchronism with the card rows (row driver 9 conducts as card row 9 is at the read brushes, and so forth for the whole card). When a read brush

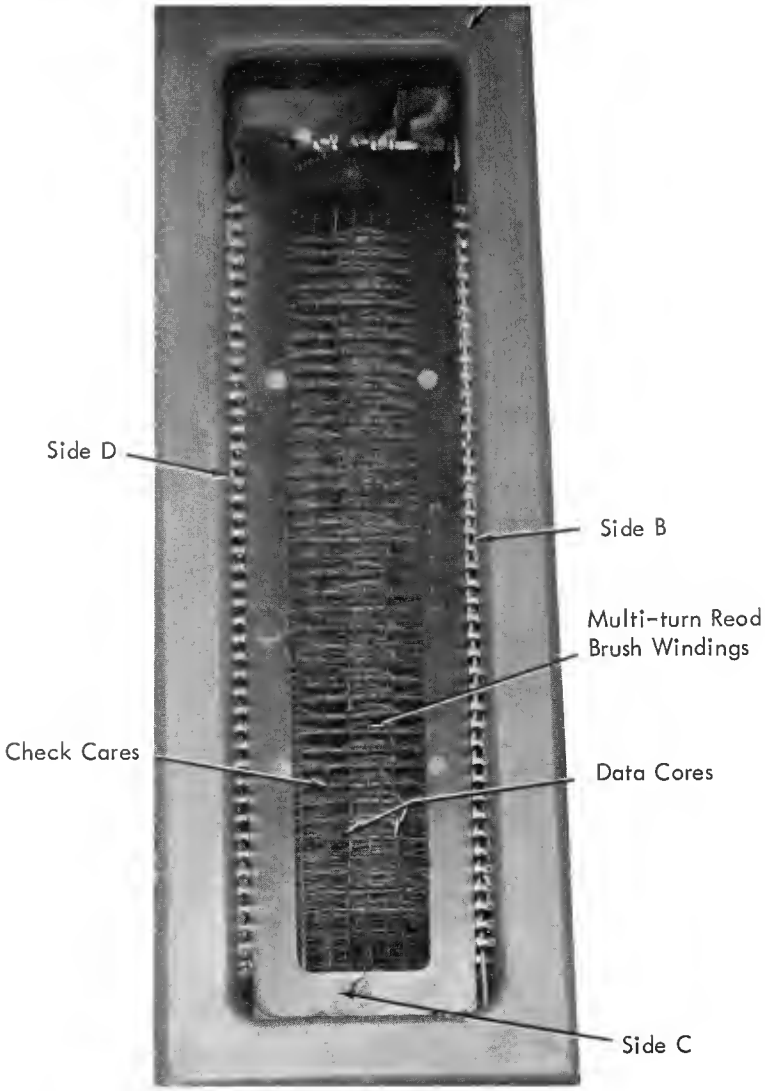


FIGURE 5.1-1. CORE ARRAY (TOP VIEW)

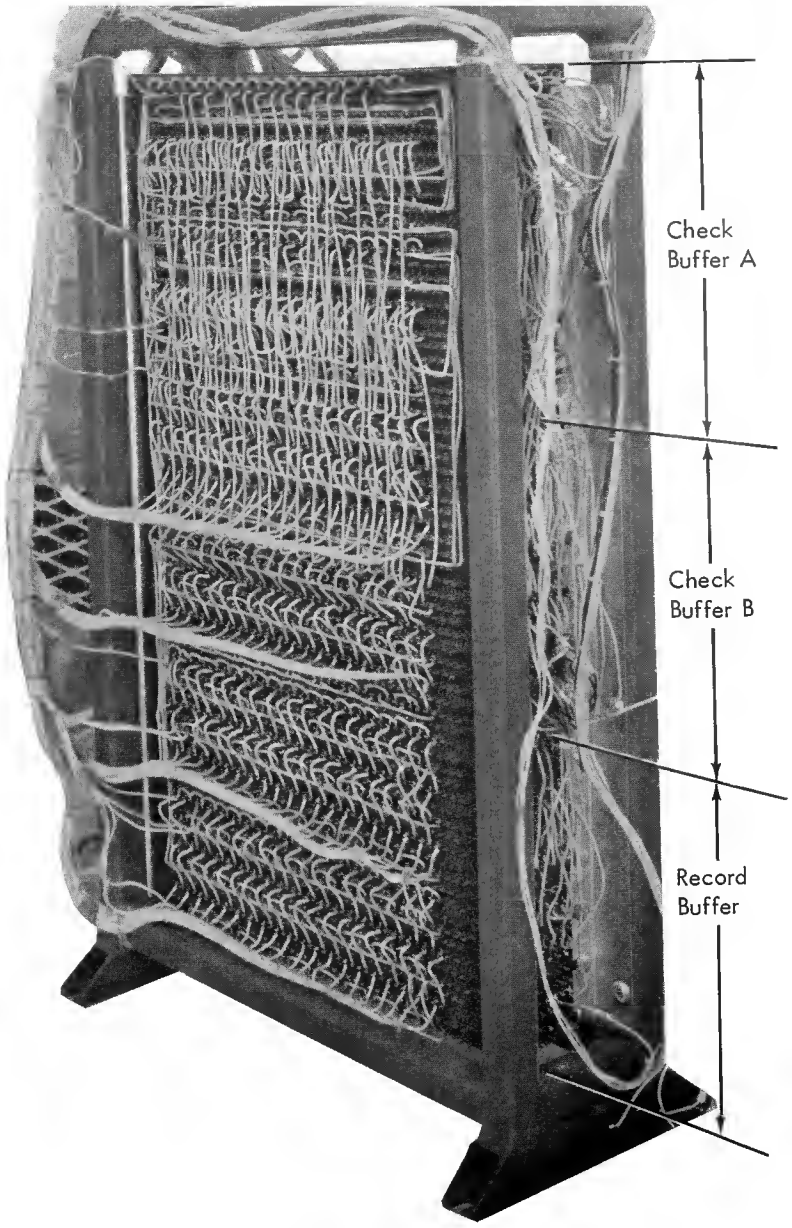


FIGURE 5.1-2. CORE ARRAY

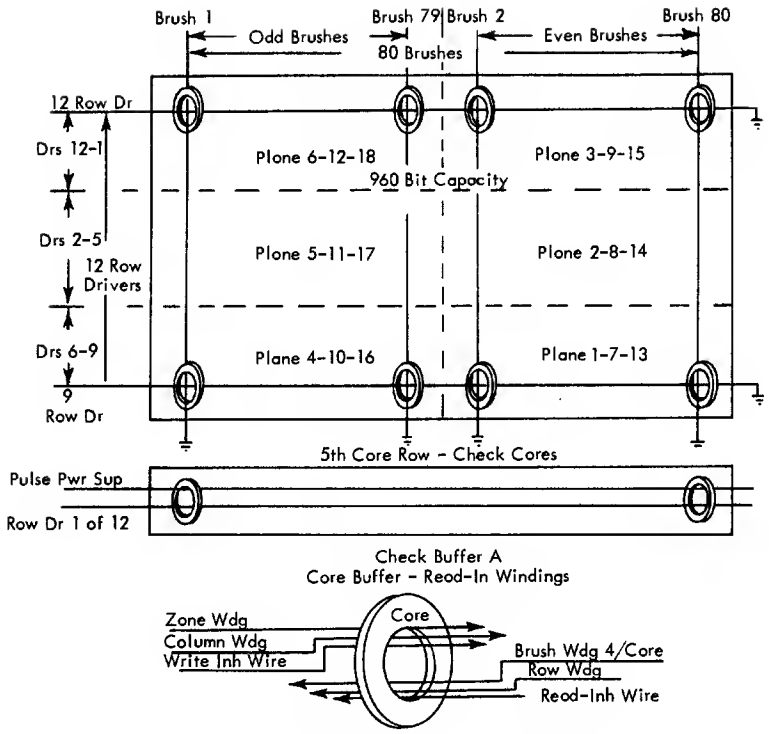


FIGURE 5.1-3. WIRES THROUGH CORES

senses a punch in the card, write current flows through the corresponding brush winding (through twelve cores). Simultaneously, the appropriate row driver conducts and the coincidence of the row driver half-write current and the brush winding half-write current set a particular core in the buffer. In essence, the buffer is an 80 x 12 matrix and the coincidence of the vertical write current (brush winding) with the horizontal write current (row drivers) sets a particular core.

The fifth row of cores of the twelve core planes in the check buffers A and B are set during the card read cycle. One of the twelve row drivers supplies half write current to the fifth row of cores in each one of these planes (40 cores). The pulse power supply provides half-write current to the check cores in all the twelve planes. Therefore, as each row driver is energized, the complete 40 check cores in the corresponding plane are set. Should any row driver fail, the check cores for that plane are not set, and an error is detected during read-out. The row driver that sets the check cores in each plane is:

Core Plane	Row Driver
1	4
2	8
3	7
4	6
5	2
6	12
7	5
8	9
9	0
10	1
11	3
12	11

The apparent indiscriminate assignment of the row drivers to the core planes results from an expedient core array wiring format. Figure 5.1-3 shows the core wires and their related position through each core.

5.1.3 Principles of Core Buffer Read-Out

The previous section explained the wiring layout to the core planes necessary to obtain an 80-bit read-in when a card is read. Similarly, a unique read-out writing layout is required to transmit data from each buffer in eight bit bytes.

The buffer read-out is controlled by ten zone drivers and twelve column drivers that combine to provide read-out current to the buffer cores. The zone and column drivers each supply one half core read current. By combining the twelve column drivers with each of the ten zone drivers, 120 read-out combinations result for buffer read-out. The operation is started by a read instruction. Zone driver 1 and column driver 1 are turned on to read the first byte from the buffer. The functional operation to read out the second byte initiates a column driver advance and provides a column 2 pulse. Zone driver 1 was not affected during this operation, so zone driver 1 and column driver 2 coincided to read out byte 2. However, as the column drivers are advanced to column driver 12, the succeeding byte read-out operation will reset the column drivers to 1 and advance the zone drivers to 2. This operation continues until zone driver 10 and column driver 12 coincide. At this time a signal is generated to indicate the end of buffer read-out.

In the read-out wiring layout, the core planes of each of the buffers are effectively arranged in parallel as shown in Figure 5.1-4. The column and zone read-out lines are threaded through two core planes in the five core direction at each buffer. These read-out lines extend through the three buffers (six core planes). At any read-out time, the data cores of one of the check buffers are inhibited to prevent data read-out. The check cores for these core planes, however, are not inhibited. When the zone and column drivers are activated, data are read from two buffers, a check buffer and record buffer. The check cores, at each byte, are read from the four check core planes.

The check cores are set by the row drivers, with one row driver supplying half-current to the 40 cores of the fifth row of cores in a plane. The fifth row of cores of the twelve core planes that make up the check buffer A and B, are supplied by one of the twelve row drivers with half-current. The row driver to core plane assignment is shown in Figure 5.1-4. The buffer read-out wiring is shown in Figure 5.1-5 with column and zone driver lines paired through each vertical column of cores. Only ten core columns are shown in the Figure 5.1-5 in each pair of core planes; but each pair of planes contains 40 core columns or data bytes. Each of the ten zone drivers is fed to each of the three pairs of core planes. The column driver, on the other hand, is specifically assigned to each pair of core planes as follows:

Column Drivers	Core Planes		
	Check Buffer A	Check Buffer B	Record Buffer
1, 4, 7 and 10	5 and 6	11 and 12	17 and 18
2, 5, 8 and 11	3 and 4	9 and 10	15 and 16
3, 6, 9 and 12	1 and 2	7 and 8	13 and 14

The ten zone drivers and the four column drivers are paired to obtain 40 read-out combinations, one for each vertical core column. The sequence of data byte read-out, however, is such that a byte is read from each pair of planes successively. Hence, the core planes 5 and 6, for example, read out data bytes 1, 4, 7, 10, 13, 16, 19, ----115, and 118. Figure 5.1-5 shows the combination of the zone and column drivers for the first two zones and the combination of the last six data bytes. The data byte number associated with the zone and column driver combinations are:

Zone	Column	Byte Number
1	1-12	1-12
2	1-12	13-24
3	1-12	25-36
4	1-12	37-48
5	1-12	49-60
6	1-12	61-72
7	1-12	73-84
8	1-12	85-96
9	1-12	97-108
10	1-12	108-120

As shown in Figure 5.1-4, the zone and column drivers are wired to all the relative core positions in the three buffers. Thus, when any zone and column driver combination conducts, the three buffers are affected. At any read-out time, however, the data cores of one of the check buffers (alternately B and A) are inhibited. Consequently, only two bytes of data are read out; from the record buffer and from one check buffer. Figure 5.1-6 is a simplified drawing of the read-out operation.

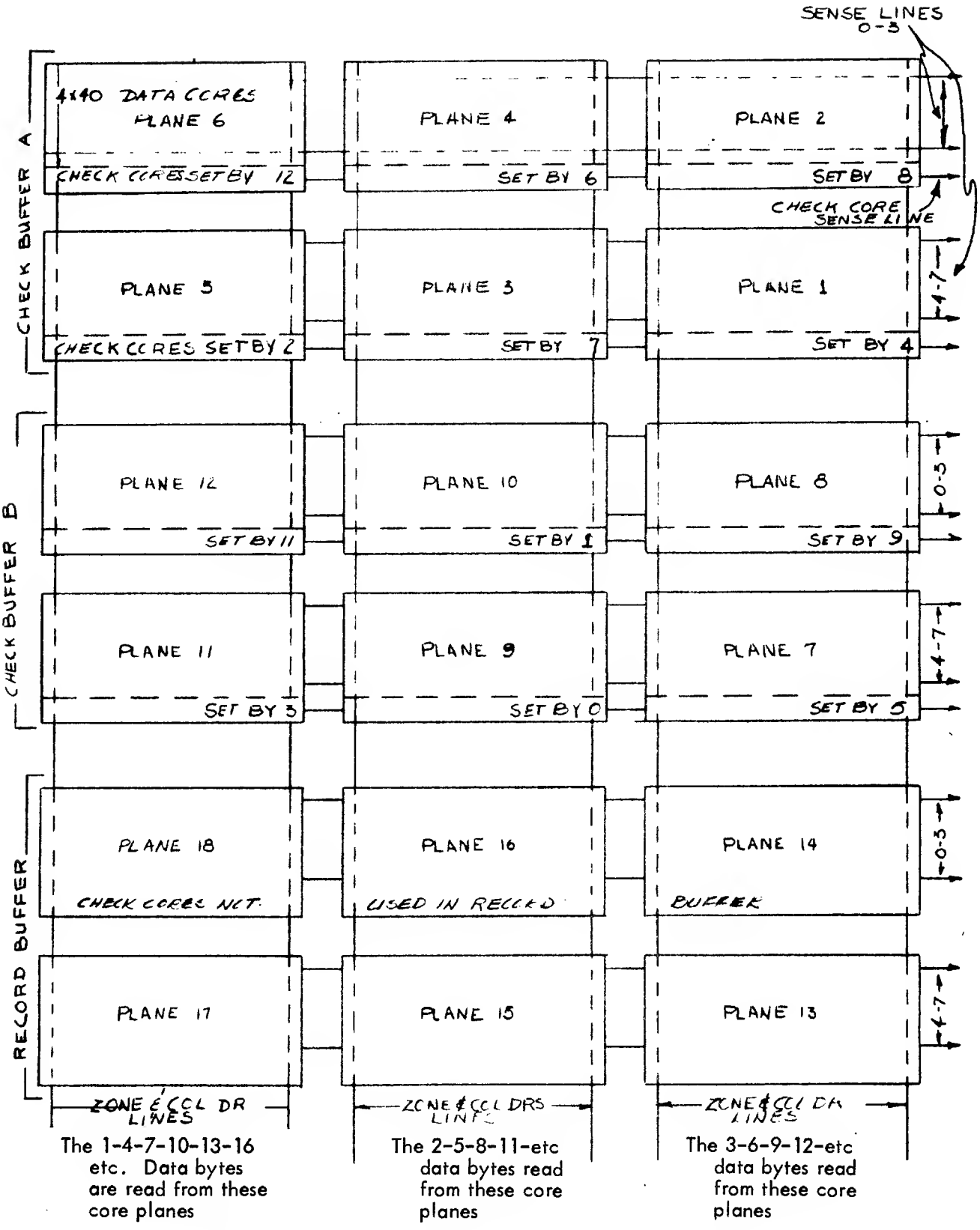


FIGURE 5.1-4. READ-OUT CONFIGURATION OF BUFFERS

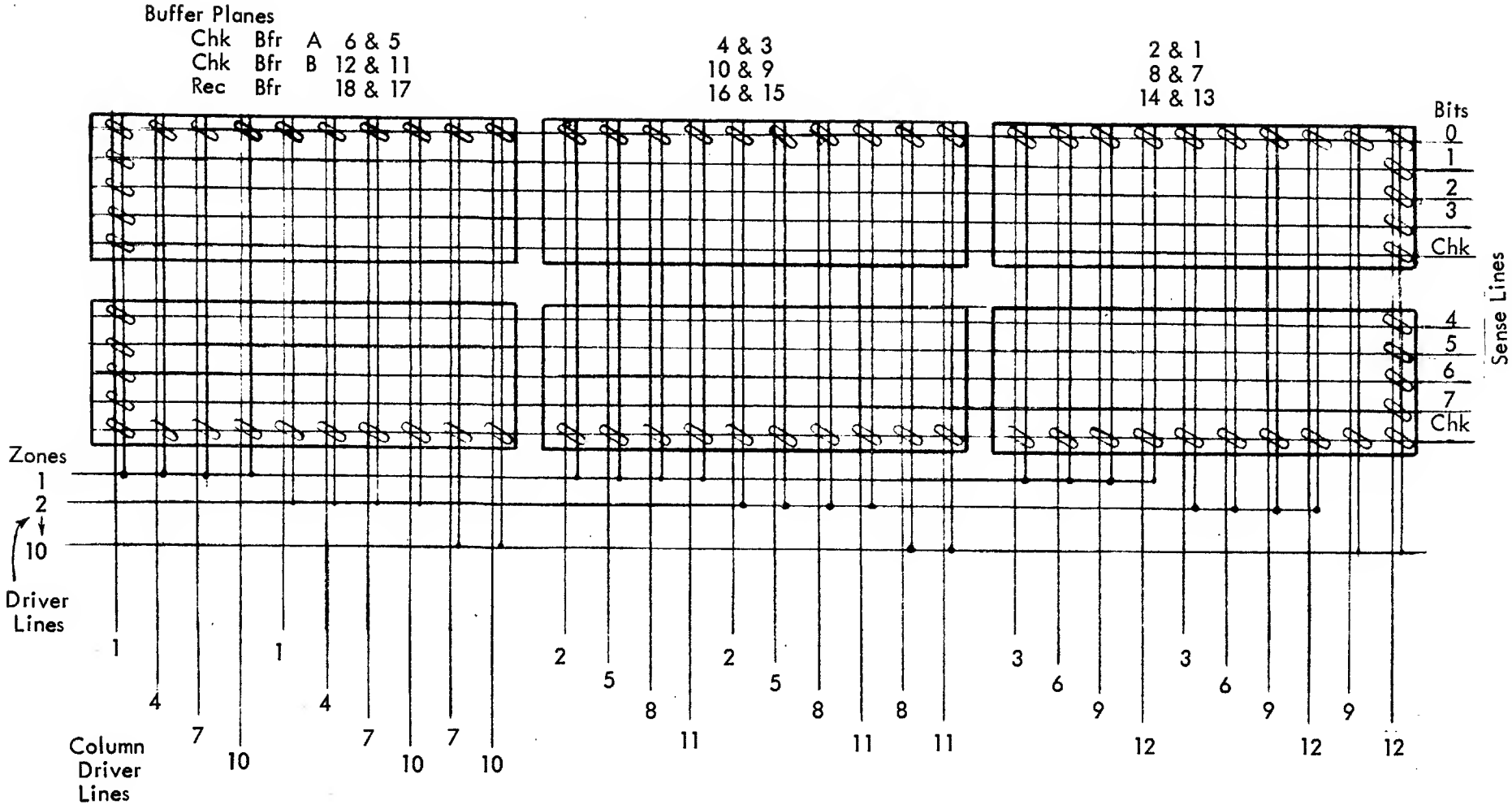


FIGURE 5.1-5. CORE BUFFER READ-OUT

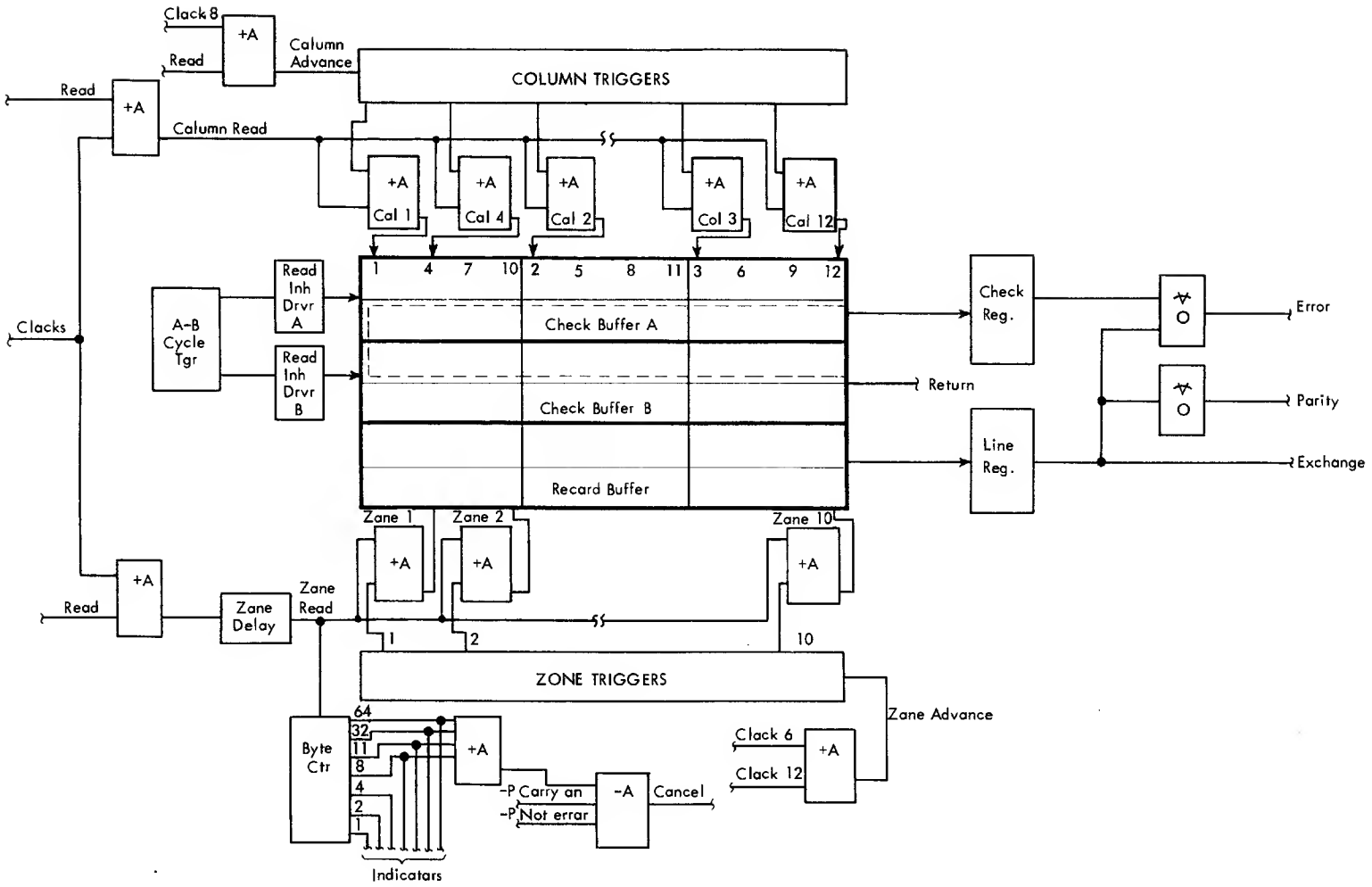


FIGURE 5.1-6. CORE BUFFER READ-OUT CARD READER

5.2 EIGHT-STAGE CLOCK

The reader control unit contains various functional devices that govern or check the operation of the control unit. These functional units, their operation and their purpose in the control unit are presented in the following text.

The eight-stage clock (Systems 01.00.01.1) provides the basic electronic control of the reader control unit. This clock consists of eight triggers tied in ring fashion and is driven by a 64 kc free-running oscillator. The go clock trigger controls the clock start and stop. The go clock trigger and the output of the 64 kc oscillator are ANDed together to provide the clock stepping sequence. Any one of three input signals (run-in-1-2-3, early disconnect, and response) turns the go clock trigger on. Once the card reader has been started, the response signal is the prevalent start control. The go clock trigger is reset by a clock 5 pulse if the service request trigger is on. When this occurs, the clock ring stops with clock trigger 4 and 5 conducting. The oscillator and go clock are ANDed at 2B (Systems 01.00.01.1) and furnish an in-phase and out-of-phase output pulse.

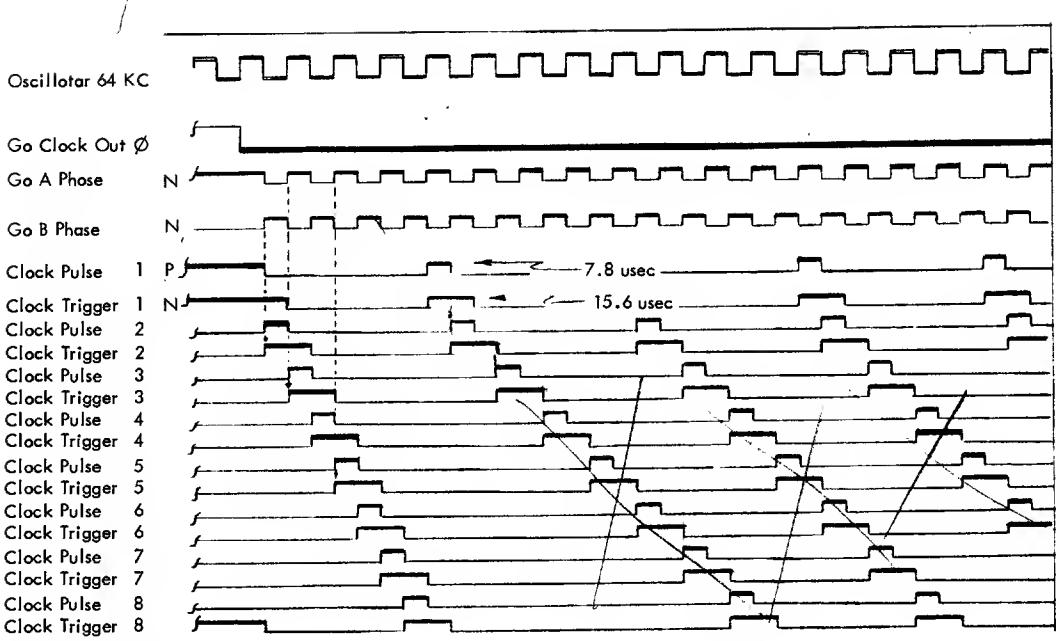
The eight-stage clock consists of eight AND input blocks and eight clock triggers. The machine reset line resets the go clock and clock triggers 1 through 7 off and turns on trigger 8. With the go clock trigger turned off, the output of the AND circuit at 2B (Systems 01.00.01.1) is a constant plus signal on the in-phase line. Consequently, the input to the clock 1 trigger is conditioned and the trigger turns on. In a reset state, therefore, clock 1 and 8 triggers are on. During normal operation two clock triggers are on at every clock pulse.

Figure 5.2-1 depicts the sequential operation of the eight stage clock. The in-phase and out of phase lines from block 2B (Systems 01.00.01.1) are specified as go A phase and go B phase respectively. The go A phase line activates the odd clock triggers and the go B phase turns on the even triggers. This arrangement makes use of the plus and minus levels of the 64 kc oscillator output and the clock steps for each oscillator shift. The clock advances by ANDing a go phase line with the preceding clock trigger. As the clock triggers turn on, the in-phase line conditions the succeeding trigger AND block, and the out-of-phase line resets a previous trigger (the second trigger behind the current trigger being turned on). The clock pulses are 7.8 usec in duration and the clock triggers are on for 15.6 usec when the clock is operating.

5.3 READ-OUT DELAY CIRCUIT

The read-out delay circuit (Systems 05.00.03.1) consists of two single-shot oscillators that delay the buffer read-out control line. This delay is necessary because a possible confliction of the buffer read-in circuits with the read-out circuits exists. During a card feed cycle, the 209^{o} - 212^{o} magnetic emitter pulse (in the card reader) initiates the buffer read-out control line. However, 209^{o}-212^{o} is read time for the 12 punch in the card at the card reader. Thus, the read-out control must be delayed until buffer read-in is finished and the read-in circuit has returned to an inactive state.

The delay circuit includes the 209 delay single-shot, with a delay factor of 700 usec, and a read-out delay single-shot with a 100 usec delay. These single-shots operate serially. The 209 delay is triggered first, and as it times out, the read-out delay is triggered. The 209 delay single-shot ensures that the brush drivers and the inhibit drivers retain their control during the buffer write operation (12 punch reads at 209^{o}-212^{o}). The read-out delay single-shot provides substantial time for the write lines



Note: Clock 1 through 8 are reset on Systems
01.00.01.1
01.00.02.1
01.00.03.1

FIGURE 5.2-1. EIGHT-STAGE CLOCK

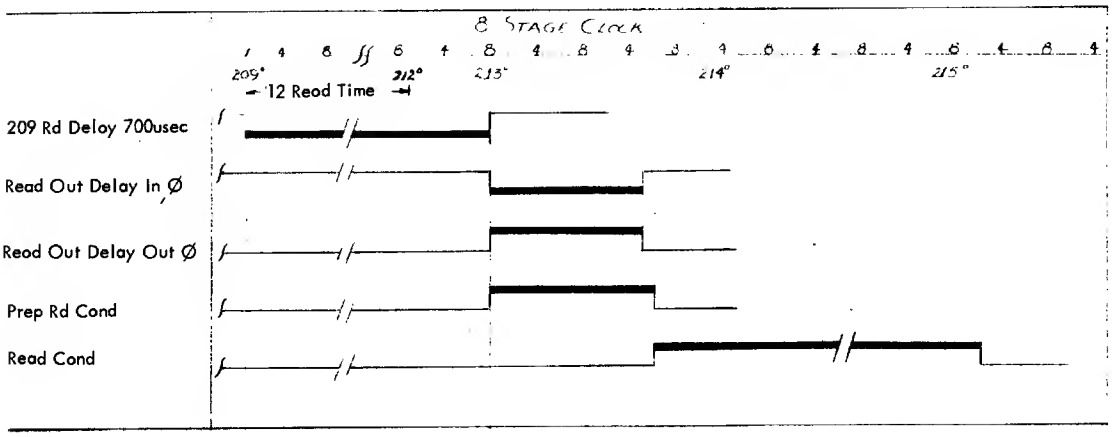


FIGURE 5.3-1. READ DELAY

to become inactive before the read-out operation at the buffers starts.

A sequence chart of this delay operation, Figure 5.3-1 shows the operation of the delay single-shots. This chart shows the relationship of the two single-shots to the pulses generated by the magnetic emitter. When the 209 delay single-shot is triggered on, the 700 usec delay (4.2 degree delay) detains the read-out control beyond the 12 card read time; the 12-time pulse from the magnetic emitter is 500 usec long. The read-out delay single-shot is triggered as the 700 usec single-shot times out and the in-phase line of the read-out delay trigger shifts to reset the brush drivers. Simultaneously, the out-of-phase line goes plus and the prepare read condition latch is turned on. This 100 usec pulse provides enough time to return the brush driver and the inhibit write circuits to an inactive state. With the timing out of the 100 usec single-shot, the read condition trigger is turned on under the following conditions: read latch on, clock 6 pulse, and prepare read condition on. The read condition latch resets the prepare read latch to necessitate a delay operation for the succeeding read operation. If normal buffer read-out results, the read condition single-shot is reset at the carry pulse and clock 4 time.

5.4 A-B CYCLE AND INHIBIT DRIVERS

The A-B cycle control trigger (Figure 5.4-1, Systems 03.00.06.1) guides data read at the first read station into the proper check buffer. The data compare feature of the reader control unit compares the data read at the first and second read stations from the same card. Data read at the first station must be retained until the same card data are entered into the record buffer from the second read brushes. To accomplish this data delay, two check buffers are designed to accept information read at the first read station. Thus, as one card reads into one check buffer, the other check buffer contains the data of the previous card and is compared with the record buffer in the subsequent read-out operation.

The check buffers A and B are directly controlled by the inhibit drivers, which are controlled by the A-B cycle latch. Four inhibit drivers, two for check buffer A and two for check buffer B, are utilized as check buffer controls. The combination of the A-B cycle trigger on or off output with either a read condition line or brush driver 1 output governs the inhibit drivers that conduct.

During the buffer write portion (buffer read-in) of a card cycle, the A-B cycle trigger and brush driver 1 will conduct one of the two write inhibit drivers and determine the buffer that is loaded. Similarly, during the read operation (buffer read-out), the coincidence of the A-B cycle trigger and the read condition trigger determines the buffer to be read. The following chart shows the situation for buffer control.

A-B Cycle Latch	Inhibit Write Dr	Inhibit Read Dr	Write Buffer	Read Buffer
ON	B	A	A	B
OFF	A	B	B	A

With the A-B cycle trigger turned on during a card reader cycle, the check buffer A is read in and check buffer B is read out. Conversely, with the A-B cycle trigger off, the check buffer B is read in and the check buffer A is read out. Hence, the alternating condition of the A-B cycle trigger determines the check buffer that writes and

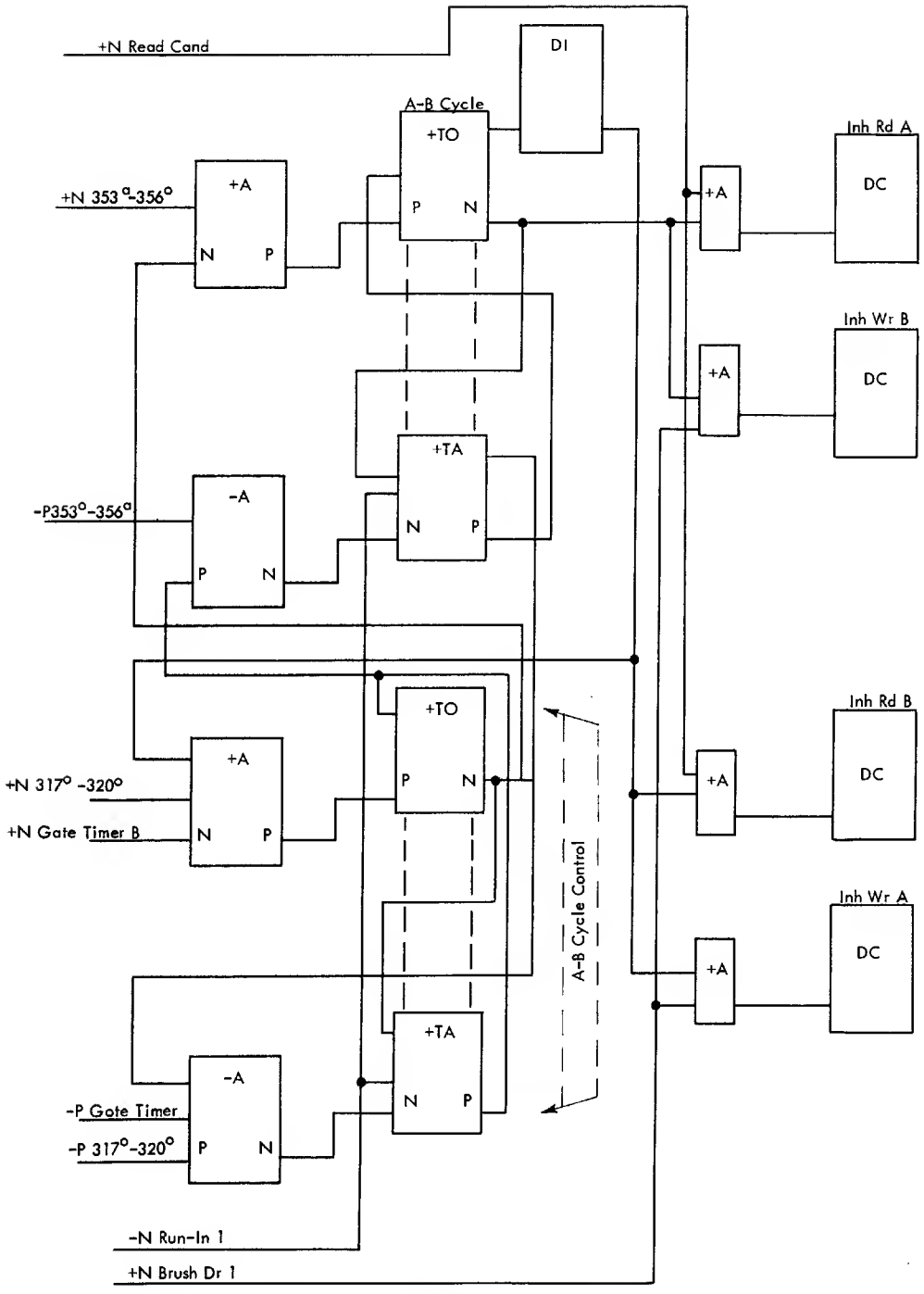


FIGURE 5.4-1. CARD READER A-B CYCLE

reads during a card cycle. The A-B cycle trigger is turned on during the second card feed run-in cycle and alternates off and on for each subsequent card cycle.

Figure 5.4-1 represents a logic diagram of the A-B cycle trigger and the control of the inhibit drivers. The cycle trigger is held reset during the first card run-in cycle of the run-in operation. The control trigger is conditioned to turn on at 317^{o}- 320^{o} of the second run-in cycle. At the beginning of the second run-in card cycle the A-B cycle trigger is turned on at 353^{o} - 356^{o} and the inhibit driver (inhibit write B) is energized to prevent read-in to check buffer B (check buffer A reads in). During the buffer read portion of run-in cycle 2, the buffer read operation does not occur, because the read condition trigger is not turned on.

Similarly, at the beginning of the third run-in cycle, the A-B cycle control trigger is turned off and the A-B cycle trigger turned off at 353^{o}-356^{o}. Under the off condition of the A-B trigger, inhibit driver A is energized and the second card reads into check buffer B. Simultaneously, the first card is read at the second brushes and the card data are entered into the record buffer. The read portion of this third run-in cycle permits a read operation, if a read is instructed from the exchange. The read condition latch is turned on, and in association with the A-B cycle trigger off, allows the check buffer A to read out. Thus, the A-B cycle trigger alternately controls the inhibit drivers and these drivers define the read-out and read-in format of the check buffers.

5.5 PARITY CIRCUIT

The parity circuit (Figure 5.5-1, Systems 04.00.03.1 and 04.00.04.1) has a twofold purpose. First, this circuit is used to generate a parity bit for each byte (eight bits) of data transmitted to the exchange, and secondly, this circuit parity checks the control function code received from the exchange during a control operation. Odd parity is used in all I-O units.

The data transmission, from the reader control unit to the exchange, is accomplished in eight-bit bytes plus a parity bit with each byte. This parity bit is handled at the exchange to ensure that the data byte was transmitted without error. To generate the parity bit in the reader control unit, the eight data bits from the line register are entered into the parity circuit to determine an odd structure of bits. If the byte has an even bit structure a parity bit is transmitted to the exchange and conversely, should the bit structure be odd, a parity bit is not sent to the exchange in parallel to the eight data bits. With the reception of a data byte at the exchange, another parity circuit samples the eight-bit byte and genrates a parity bit. This parity bit generated in the exchange is compared with the parity bit sent from the reader control. An equal condition between the parity bits designates satisfactory transmission.

When a control operation is initiated, the control function code is parity-checked as the code enters the line register in the reader control unit. A parity bit is also sent from the exchange with the control code if the code has an even bit structure. This function code in the reader control unit generates a parity bit and this generated parity bit is compared with the transmitted parity bit. If the two parity bits are equal and the function code is valid, the code initiates the desired function. However, should the parity bits disagree, the unit check trigger in the reader control unit will signal an error.

Figure 5.5-1 is a logic diagram of the reader control parity circuit. The left half of the figure is the parity tree found on Systems 04.00.03.1 and the right half is the parity

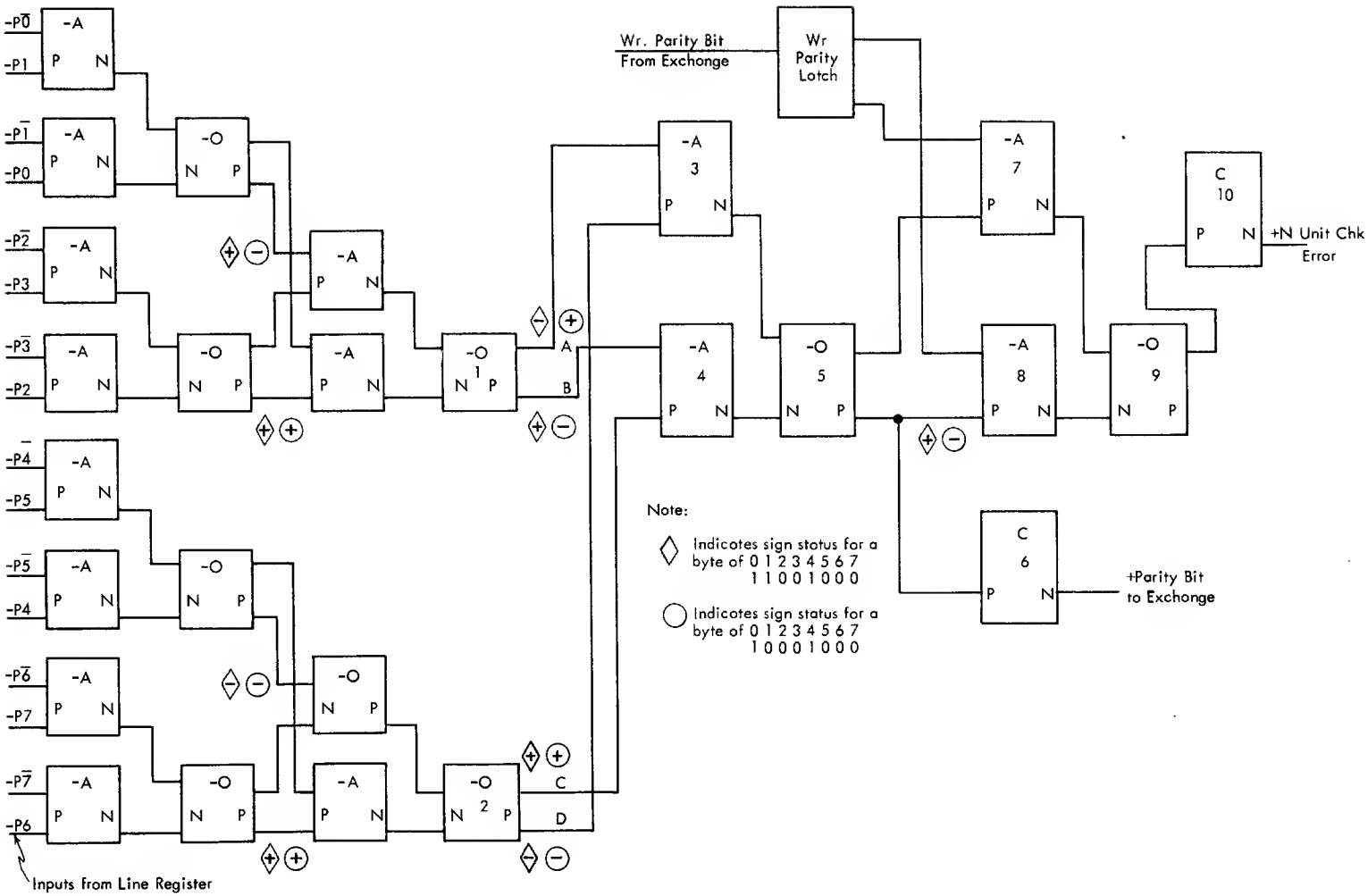


FIGURE 5.5-1. PARITY CHECK AND BIT GENERATION

generator and error circuit found on Systems 04.00.04.1. The inputs to the parity circuit are provided by the line register. Blocks 1 and 2 are the outputs of the two identical halves of the parity tree. The signs indicated in the diamonds represent the in-phase and out-of-phase line levels for a byte of

```
0 1 2 3 4 5 6 7
1 1 0 0 1 0 0 0  (ODD)
```

Assume that these signs (enclosed in the diamonds) are available and that a normal read is in progress (for an explanation of the circuit to the right). Thus, block 4 has 2 plus inputs; hence, a plus output. Block 3 has 2 minus inputs; hence, a minus output. Because block 5 is a -OR, its output is minus at this time for the in-phase line, and plus for the out-of-phase line. No parity bit is generated in this case, because the bit structure of the byte is odd. During this parity operation, the write parity trigger is off, the outputs of block 7 and 8 are plus, and block 10 has a minus output. Regardless of the output of converter block 10, the unit check is not affected during a data transmission parity generation. This error line to the unit check is permitted to set the unit check during a control operation only.

The signs indicated in the circles represent the parity tree output when a byte of

```
0 1 2 3 4 5 6 7
1 0 0 0 1 0 0 0  (EVEN)
```

is entered into the parity circuit. By starting with these signs and following the circuit to the right, the output at block 5 is found to be plus on the in-phase line. Consequently, the parity bit line is plus through converter 6, and a parity bit is transmitted with the byte to the exchange. Thus, an odd number of bits is sent to the exchange during every transmit operation.

The second purpose for the parity circuit is to check the control instruction sent from the exchange during a control operation. During a control operation, the function code is entered into the line register in the reader control unit. The parity bit associated with this function code is directed to the write parity trigger. As previously shown, all data transmitted are in odd parity. If the function code bit structure is even, a parity bit accompanies the code.

To show the error detection feature of this circuit, assume that the function code has lost a data bit and that the parity bit is present. Because the parity is present, the original function code contained an even bit structure at the exchange. Now the data bit structure is odd with a parity bit.

As the function code enters the line register (odd number of bits), the outputs at blocks 1 and 2 are as shown in the diamonds. Hence, the outputs at block 5 are minus at in-phase line and plus at the out phase line. Concurrently, the write parity trigger is turned on by the parity bit from the exchange. Therefore, the inputs to block 8 are both minus and the output is plus. The out-of-phase output of block 9 (with this situation) is plus, and the error line is raised. Because the reader control unit is performing a control operation, the error line is allowed to set the unit check trigger.

5.6 COLUMN AND ZONE DRIVER OPERATION

Twelve column and ten zone triggers (Systems 03.00.09.1 through 03.00.16.1) provide driver outputs that are combined to develop 120 read-out pulses. These read-out pulses are fed to the three core storage buffers, simultaneously. The column and zone triggers are tied in a ring fashion and are advanced, independently. The zone advance circuit is conditioned by column driver trigger 12 turn-on, and the zone advance occurs only when this gate is present. The column advance is controlled by a read operation or by a flush operation. The flush operation occurs during the run-in cycle 1 and clears the core storage buffers before the buffers are loaded. The inhibit drivers to the check buffers are not active during a flush, and, therefore, check buffers A and B and the record buffer are cleared.

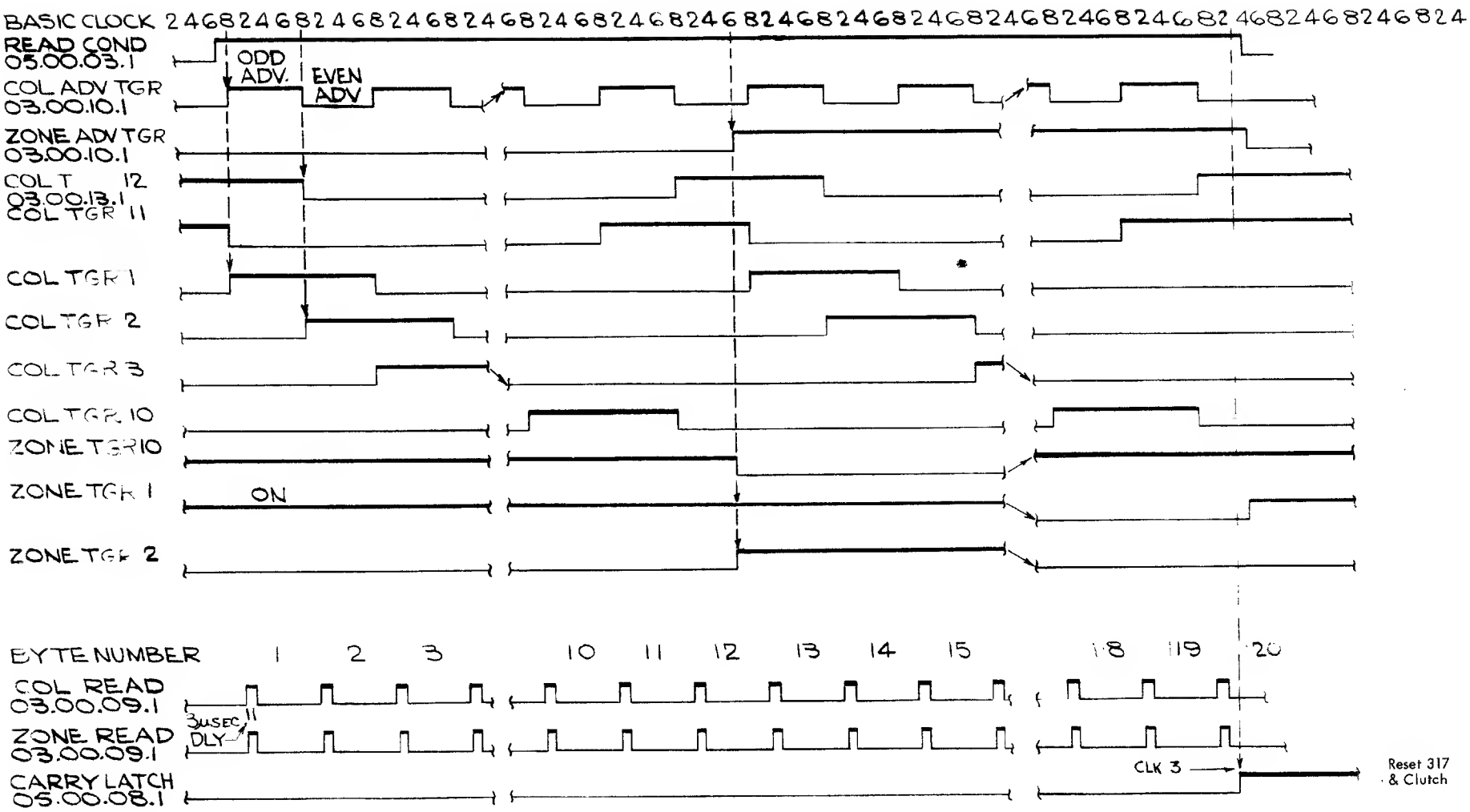
The column and zone rings are advanced by their respective advance triggers turning on and off (Systems 03.00.10.1). The odd and even numbered zone and column ring triggers are turned on by their advance trigger as follows:

Column advance trigger off -- advance even ring triggers.
Column advance trigger on -- advance odd ring triggers.
Zone advance trigger off -- advance odd ring triggers.
Zone advance trigger on -- advance even ring triggers.

Initially, the zone and column rings are reset with zone triggers 1 and 10 on, and with column trigger 12 on and the zone and column advance triggers off. The flush operation occurs before a read operation can be started, when the reader is made ready. This flush is started at clock 6 and conditions the AND circuits to the advance triggers. Because the zone advance trigger is turned on at clock 5 time and the column advance is turned on at clock 7, the column advance (only) turns on as the flush is initiated at clock 6.

When the flush operation is completed, the column 11 and 12 triggers are on and the zone 1 and 10 triggers are on. The core buffers are loaded during run-in cycle 2 and 3, and a read instruction will start the column and zone rings for a core read-out. Similar to the flush, the read condition is raised at clock 6 time and the column advance trigger is turned on. The zone advance is conditioned by the combination of the column 11 trigger on output and the column advance trigger on (even advance). This causes the line that turns on the column 12 trigger to permit the zone advance trigger to turn on.

Figure 5.6-1 is a sequence chart of the column and zone ring operation. The flush operation is shown, but this operation occurs on the run-in when cards are loaded, only. Because of this flush, the column and zone triggers are in a definite status at the start of a read operation. When each read operation is terminated, the column and zone triggers again are left in a definite status for the next read operation. Figure 5.6-1 shows the conditions that advance the zone ring and the zone and column read pulses. The zone read pulse is delayed 3 usec, which results in a 5 usec zone read pulse to the cores. This delay is employed to prevent noise generation when the column and zone read pulses are raised simultaneously. Figure 5.6-2 presents a logic example of one of the column or zone triggers in the rings. The trigger turn-on (+AND block) also provides the control to the driver circuit. The trigger itself serves only to gate the following stage of the ring advance. Each trigger is turned off by the second successive trigger ON output.



Notes

At the completion of the flush operation the column trigger 11 and 12 and the zone trigger 1 and 10 are on.
The column and zone advance triggers are off.

FIGURE 5.6-1. COLUMN AND ZONE ADVANCE

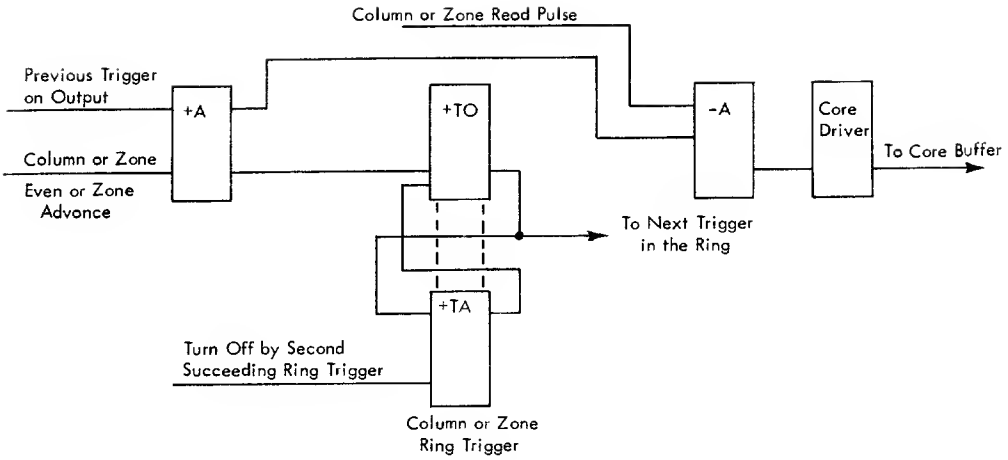


FIGURE 5.6-2. COLUMN OR ZONE RING TRIGGER

5.7 TRAP REGISTER

The trap register (Systems 04.00.10.1) is designed to accept and retain the first data error recognized during a normal read operation. If the reader control unit is in a control operation, the entry to the trap register is blocked. However, the line, check, and trap registers are all reset during the control function. While card reading is in Error Check and Correcting (ECC) mode, the trap register receives the bits in error but does not retain them.

If a data error is recognized by the compare circuit during a normal read operation, the bit in error is entered and stored in the trap register. The error bit enters the trap register at the coincidence of clock 2 and unit check latch Off. However, this same error turns on the unit check latch at clock 4. Hence, once a data bit in error is detected and entered into the trap register, the trap register is isolated from the operation. The trap register is reset when the subsequent read instruction resets the unit check trigger.

5.8 BYTE COUNTER

The byte counter (Systems 04.00.13.1 through 04.00.14.1) consists of seven negative binary triggers capable of accumulating to 127. This counter is advanced one by the zone read pulse (clock 1) whenever a byte of data is transmitted to the exchange. The purposes of this counter are:

1. To retain the number of the byte in error when a compare error is sensed during data transmission.

2. To make a ring check when the last byte of data is read from the core buffers during data transmission.

In the first situation, if a compare error is sensed and the unit check trigger is turned on, the zone read pulse is blocked from advancing the byte counter. Hence, at the end of the block of data, when the operation is terminated, the number of the byte in error is contained in the byte counter. The counter is used to make a ring check of the zone and column rings. If the counter value is less than 120 when the last byte of data is read from the buffers, a ring check is initiated. The byte counter is normally reset at 317^{0} of the magnetic emitter timer when the clutch trigger is on.

5.9 MAGNETIC EMITTER TIMING PULSES

The magnetic emitter (Systems 03.00.01.1) located in the card reader provides seventeen 500 usec pulses to the reader control. These pulses are amplified and used to synchronize the mechanics of the card reader to the circuits in the reader control. Of these 17 pulses, twelve are synchronized to the twelve rows of the data card and five are control pulses. The twelve card row pulses are gated by the reader control circuits when the data card is moved past the read stations. These twelve row pulses are ANDed with the brush drivers to generate the reading pulses. In addition, these same twelve pulses drive the 12 row drivers that feed the core buffers at each card cycle point.

5.9.1 Functions of Timing Pulses

		Systems Page
11°	9 - Gates row drivers and brush drivers during card reading	03.00.01.1
29°	8	03.00.01.1
47°	7	03.00.01.1
65°	6	03.00.01.1
83°	5	03.00.01.1
101°	4	03.00.01.1
119°	3	03.00.01.1
137°	2	03.00.01.1
155°	1	03.00.01.1
173°	0	03.00.01.1
191°	11	03.00.01.1
209°	12	03.00.01.1
245°	- Resets Run-In 3 Tgr	05.00.05.1
	Gates turn-on of Clutch Tgr (if clutch is not engaged)	05.00.04.1
263°	Gates turn-on of Run-In 3 Tgr	05.00.05.1
	Feed check - if gate timer is on	05.00.07.1
	Gates turn-on of Clutch Tgr (if clutch is engaged)	05.00.04.1
299°	Gates turn-on of Run-In 2 Tgr	05.00.05.1
	Gates turn-on of Start Tgr	05.00.06.1
	Gates reset to Gate Timer Tgr	03.00.04.1
317°	Gates turn-on of Gate Timer Tgr	03.00.04.1
	Gates A-B Cycle Control	03.00.06.1
	Gates reset to Carry Tgr	05.00.08.1
	Gates reset to byte counter	04.00.13.1
353°	Gates A-B Cycle Tgr (binary Tgr)	03.00.06.1
	Gates turn-on of Brush 1 and Brush 2 Tgrs	03.00.05.1
	Gates the reset to Drive Tgr	05.00.06.1
	Resets Clutch Tgr	05.00.04.1
	Resets Unload Tgr	05.00.01.1
119°	Resets card lever 2 Tgr	05.00.07.1
173°	Gates turn-on of Prepare Ready Tgr	05.00.06.1
	Gates turn-on of Feed Check	05.00.07.1
	Gates reset to CL 1 Latch	05.00.07.1
191°	Gates turn-on of Flush Tgr (on run-in 1)	05.00.05.1
	Gates turn-on of Feed Check	05.00.07.1
209°	Turns on 209 Delay single-shot	05.00.03.1

6 FUNCTIONAL OPERATIONS

THE CARD reader and reader control unit are capable of reading punched cards and entering these data into main memory of the 7030 System. These units perform two basic operations: (a) read operation, and (b) a functional control operation. The read operation incorporates the movement of a card through two read stations, the comparison of the data read from each read station, and the transmission of this data to the exchange. The control operation performs the following functions: reserve light On, reserve light Off, ECC mode On, ECC mode Off, and read check light On.

The right effective address of the I-O instruction that specifies a control operation, contains the binary code that determines the function performed. The operations performed by the card reader and the control unit are presented by logic flow charts. These charts consist of block representations of a machine function or operation. The Systems number that contains the logic circuitry of the represented function is shown in the block along with the function. The start function or the continuation of a previous operation are located at the top of the flow chart and the chart reads downward. The shape of a block denotes the block type. The block types and their usage are shown in Figure 6-1.

6.1 BASIC MACHINE CYCLE

The basic machine cycle of the card reader is 60 ms in duration. Card reading and data transfer occur within the basic cycle during continuous operation. The cycle starts at 315^{0} (card feed clutch latch time), card reading occurs from 11^{0} to 212^{0}, and data transfer is permitted to start at about 214^{0} of the card reader cycle. Two factors determine the continuous operation of the card reader: (1) the interval between consecutive read instructions (or the multiple flag setting in the control word) and (2) the data load on the exchange.

The maximum data load of the exchange is 67,000 bytes per second, handled at the exchange. This load is determined by the number of I-O units operated simultaneously by the exchange. To ensure that card data are not lost when the exchange reaches a maximum load condition, the data transfer of the buffered I-O units is delayed to reduce the exchange load. Because of the delay in the data transfer, the timing conditions for continuous reader operations cannot be met. The data from the control unit buffer must be transferred before 263^{0} of the card reader cycle for continuous card reader operation.

Secondly, if the read instructions are not sent to the reader control unit within minimum time intervals, continuous card reader operation cannot occur. Thus, the time interval between read instructions, and the time required to transfer data to the exchange determine continuous card read operation.

The preceding text presents the functions within a cycle that affect continuous reader operation. However, assume that the data buffers are loaded and that the card feed clutch is latched when a read instruction is received by the reader exchange channel. The buffer data transmission is started immediately. The card feed clutch, however, is energized after the buffers are read out (carry latch ON) and at 245^{0} of the card read cycle. A delay of 60 ms may be encountered before the card feed operation starts at the reader, if the read instruction were received at 246^{0} of the card reader cycle. Continuous card feed operation may then be established if the read instructions are frequent enough and

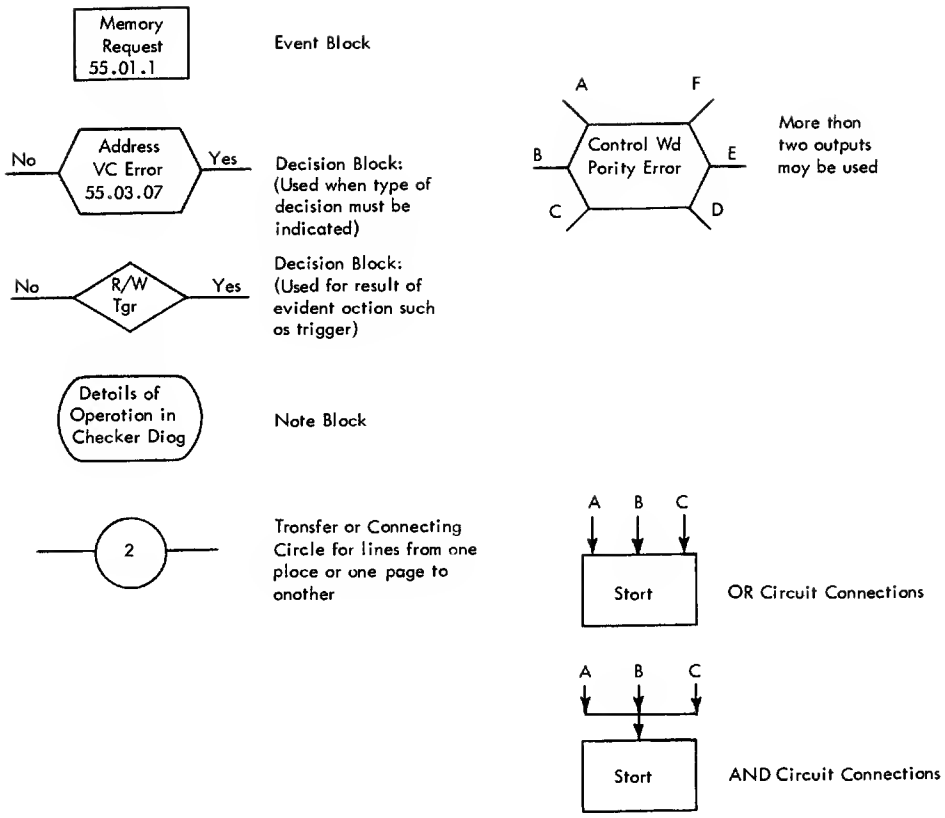


FIGURE 6-1. LOGIC FLOW BLOCKS

the exchange load is not heavy after the first card feed is started.

An additional delay in the card feed operation occurs if the reader drive motor is stopped when a read instruction is received by the control unit. This situation requires that the drive motor attain operating speed before a card feed cycle can be signalled.

A Haydon timer controls the drive motor in the card reader. If a read instruction is not directed to the card reader for a pre-set interval of time, the timer opens the drive motor circuit. The time can be adjusted for intervals between two to twelve minutes. Once stopped, the drive motor requires approximately 230 ms to attain operational speed.

Figure 6.1-1 graphically represents a basic machine cycle. The time intervals for the card read operation and the data transmission are denoted. Also, note that a card feed clutch is energized at 245° when the clutch is latched and a read instruction is received at the exchange.

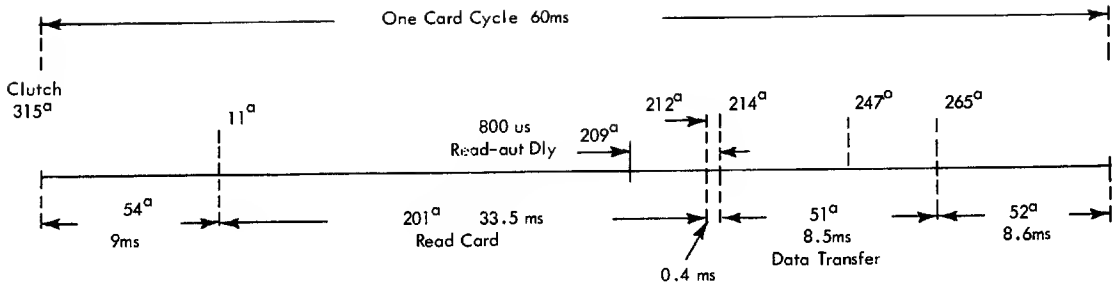
6.2 RUN-IN OPERATION

Prior to initiating any operation at the card reader, the cards must be loaded and run into the reader. This run-in operation consists of feeding three cards into the card reader, loading the buffers, and conditioning the reader to a ready status. Once the ready line is established, the card reader is operable from the main program with a read or control instruction. At the completion of the run-in operation, the data from the first card are in the buffers ready for transmission on a read instruction and this card is in the stacker.

Figure 6.2-1 is a flow chart of the first run-in cycle. Assume that the power is on and that the electronic circuits have been reset by the power-on reset. The cards are loaded in the machine face down (9 edge first) and the start key is depressed. From these functions, the various run-in 1 operations are initiated. During this run-in, any data transmission operation is blocked, the core storage buffers are cleared, and the first card feeds into the reader. Card lever trigger 1 is turned on by the card lever 1 contact. With this trigger on and at 299°- 302° of this first run-in cycle, run-in 2 cycle is initiated.

Figure 6.2-2 presents the run-in 2 cycle flow chart. The run-in 2 cycle was initiated at the end of the run-in 1 cycle and the "circle 1" indicates the connection between Figure 6.2-1 to this figure. Run-in cycle 1 trigger is reset by the run-in 2 trigger turning on. Thus, the run-in control to the go clock (eight-stage clock) and the card feed clutch trigger are not interrupted. The second card feed cycle is initiated and the first card is read at the first read station. Consequently, check buffer A is prepared to accept the data from the first card. At 353° of the second run-in cycle, the A-B cycle trigger is turned on and brush driver 1 is activated to conduct. The inhibit driver B is turned on and data are accepted into check buffer A only. The prepare read condition trigger, prepare ready trigger and end-of-message (EOM) signal are blocked during this second run-in cycle.

Figure 6.2-3 is the flow chart depicting run-in cycle 3. In a similar manner to run-in 2, the run-in 3 trigger turns on at the end of the run-in 2 cycle. The run-in 3 trigger turn-on resets run-in 2 trigger. The control to the clutch and the go clock is not interrupted. This sequencing of the run-in triggers institutes three successive card feeds. Because the card feed clutch controls card movement to the second read brushes only,



1. 1ms = 6a
2. For continuous operation, data transfer must be completed by 265a and a read instruction must be received by 214a.
3. With clutch disengaged, data transfer must be completed by 247a to initiate a card feed cycle an a READ Data transmission starts immediately, however.

FIGURE 6.1-1. CARD CYCLE

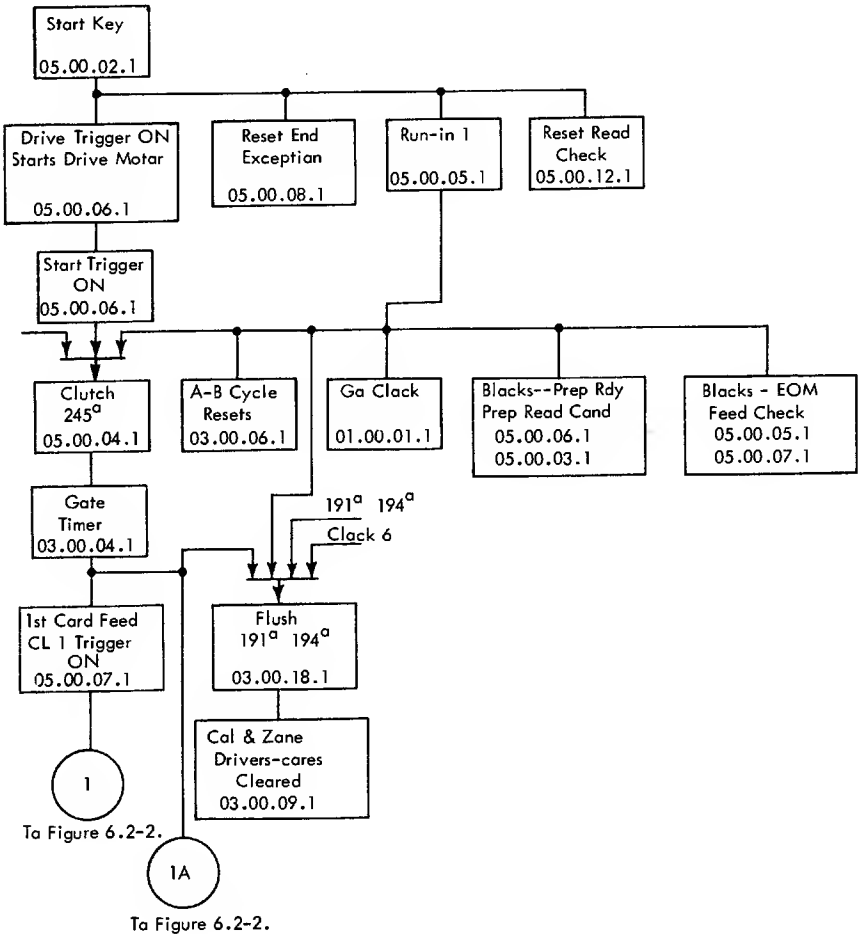


FIGURE 6.2-1. CARD READER -- RUN-IN 1

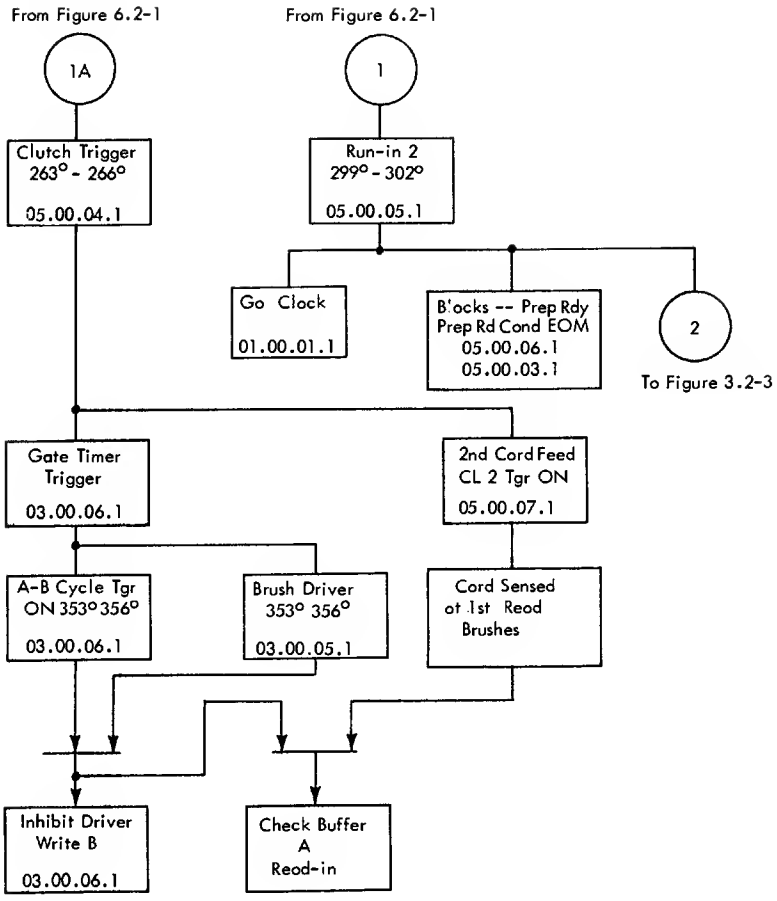


FIGURE 6.2-2. CARD READER -- RUN-IN 2

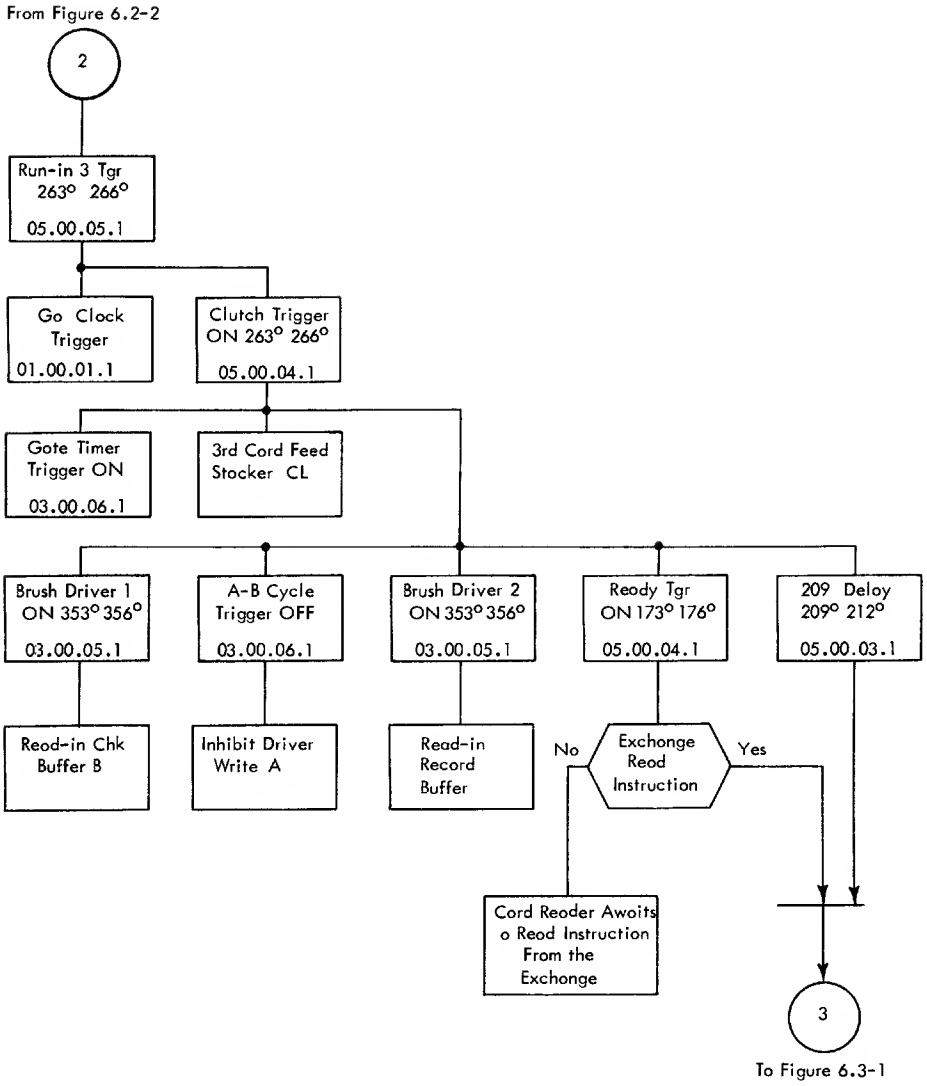


FIGURE 6.2-3. CARD READER RUN-IN 3

the first card is stacked after the three run-in cycles are completed. The data from this first card are entered into check buffer A and the record buffer.

The third run-in cycle (and subsequent card feed cycles while cards are in the hopper) must read two cards simultaneously. Because cards are moved past both read stations, during the third run-in cycle, brush drivers 1 and 2 must be conducting to sense the card data. In the previous run-in operation, check buffer A was loaded. Consequently, during this third run-in, the card read at the first read station is entered into check buffer B. Concurrently, the third run-in cycle reads the first card fed into the card reader at the second read station. These data are entered into the record buffer. (The record buffer and the check buffer A contain the data from the first card.) Toward the end of the read portion of the third run-in cycle, the ready line is activated and the read-out delay timing is started. (This read-out delay prevents the starting of a read operation before the card sensing is completed.) The ready line sets the unit ready indicator in the card reader channel control word in the exchange. A read instruction from the machine program can be accepted by the exchange when the ready status is established. However, the read operation is delayed until the read condition trigger is turned on in the reader control.

Figure 6.2-4 demonstrates the sequence of events of the run-in operation. Run-in 1 is started with the start key, and as the first card feeds into the card reader, card lever 1 is activated. Card lever 1 and card lever 2, in conjunction with the magnetic emitter pulses, step the run-in operation. The ready trigger and prepare read condition trigger are on. The ready trigger permits the exchange to accept a read instruction from the main program; the prepare read condition trigger conditions the turn-on gate to the read condition trigger. The read condition trigger turn-on starts the read operation in the reader control unit.

6.3 READ OPERATION

The card reader is under program control once the run-in has been completed. The ready status of the reader is indicated in the control word at the exchange, and if a read instruction is directed to the reader channel, the read operation results.

Figure 6.3-1 is a flow chart of the read operation. The read condition trigger is turned on by the read instruction and the trigger initiates data transmission to the exchange. (If the drive motor is stopped at this time, the motor is started, which results in an approximate 230 ms delay.) The data are transmitted from the record buffer and one of the check buffers reads out one byte of data, which is entered into the line register and check register, respectively. While this byte is in the registers, a compare check is made on the data. At clock 2 time a service request is triggered to the exchange requesting the exchange to accept the data on the line (from the line register). These data from the line register are also fed to a parity generating circuit. If the bit structure of the transmitted byte is even, a parity bit is transmitted with the byte; otherwise, no parity bit is generated. Hence, the exchange accepts the byte with an odd bit structure and initiates a byte response. This response signal controls the go clock trigger and allows the eight-stage clock to continue cycling. If the response signal is not sent from the exchange, the eight-stage clock stops at clock 5 and data transmission is suspended until the response is received, thereby starting the clock again.

Should the clock run continuously, data bytes are read out at 62.4 usec intervals until the buffers are emptied. The carry trigger is turned on during the last byte to terminate the current data transmission. The carry trigger is turned on when column driver 12, zone driver 10, and clock 3 pulse coincide. This trigger gates the read condition

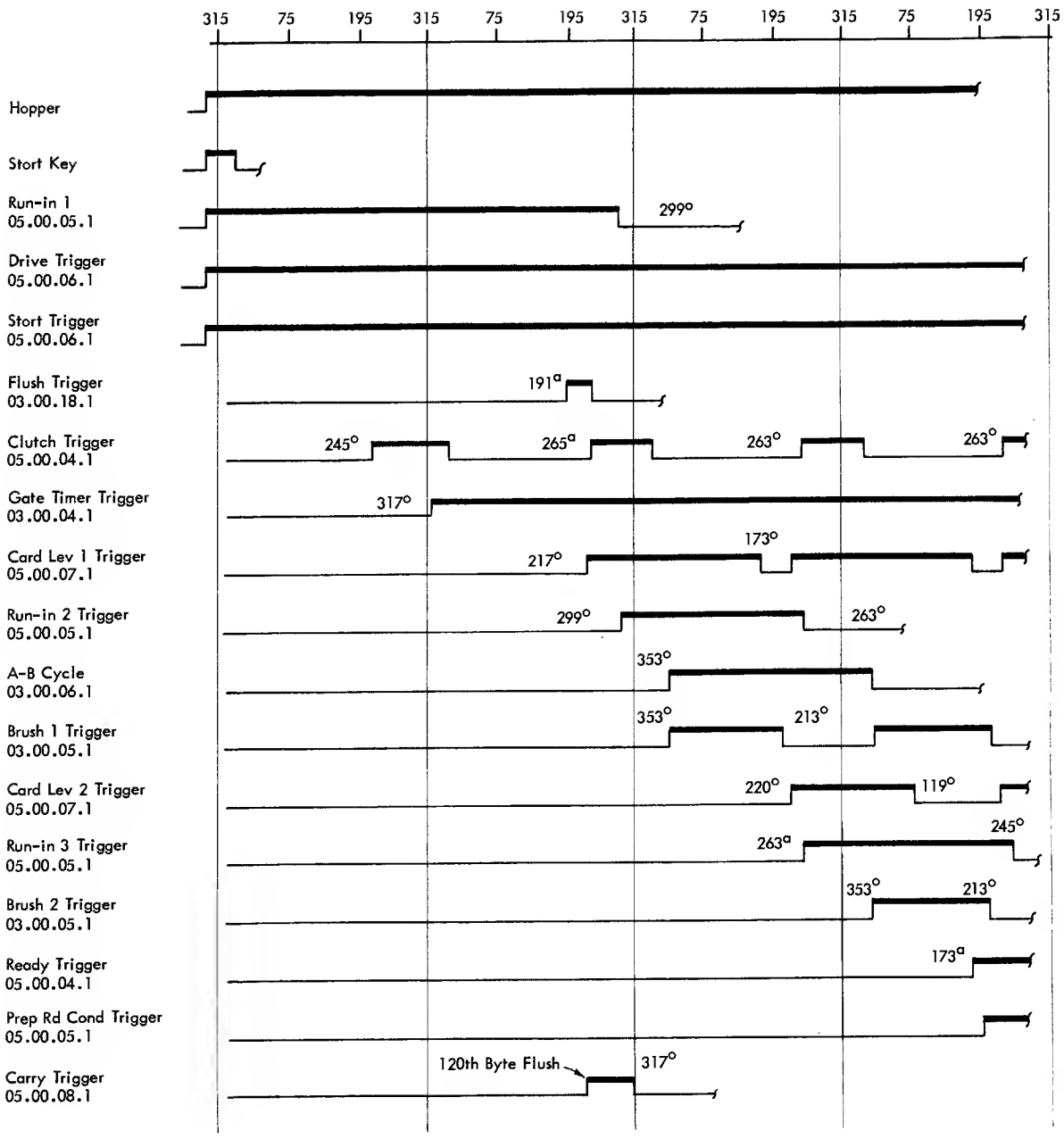


FIGURE 6.2-4. CARD READER RUN-IN SEQUENCE

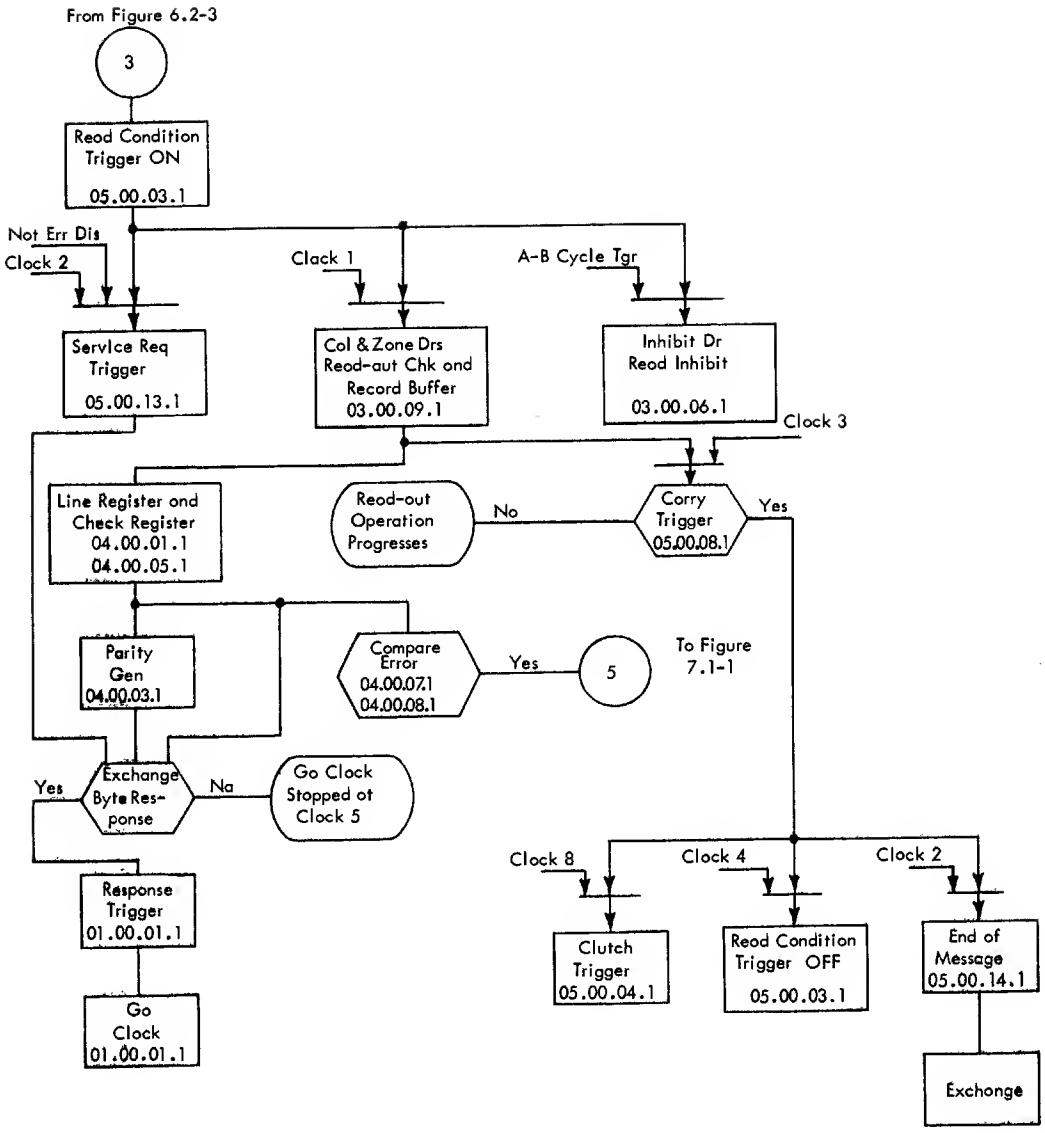


FIGURE 6.3-1. CARD READER -- READ OPERATION

trigger Off at clock 4 time terminating the read operation. The card reader clutch is energized when the carry trigger is on, to initiate a card feed cycle. This card feed reloads the buffers with the next card in preparation for the next read instruction. Finally, the exchange is signalled that the end of the current message has been reached.

During the read operation the check sense cores are also read out and their outputs are sensed at the driver check circuit.

If the compare circuit senses an unequal condition between the data in the record buffer and the data in the check buffer, the unit clock trigger is turned on. "Circle 5" indicates the compare circuit output at the unit check. This check circuit is described in subsequent check explanations. However, when a compare error is detected, the data transmission is not terminated. The unit check indication is set at the end of the current block being transmitted.

The eight-stage clock provides the basic read-out control once a read instruction is accepted at the exchange. The exchange and the card reader control "crosstalk" with service request and byte response signals when data transmission is in progress. This type of operation permits the exchange to control the rate of data transmission from the reader control unit. Consequently, the possibility of overloading the exchange channel with data is non-existent, because transmission may be suspended on an overload condition.

Figure 6.3-2 shows the sequence of the read operation for one data byte. The coincidence of the column read and zone read pulse results in a data byte read-out of the buffers. The byte is entered into the line register, and as the service request trigger turns on, the data is accepted at the exchange. The response trigger is turned on from the exchange to continue to the eight-stage clock and, therefore, the read operation.

6.4 CONTROL OPERATION

The control instruction executed by the reader control permits any of five functions to be performed at the card reader. During a control operation, data flow is from the exchange to the reader control. However, only one eight-bit byte is required to define a control function. The byte is decoded by the reader control and the function is performed at the card reader. The five functions and their respective codes are:

Name	Function Code (bits on write lines)								Write Parity Tgr
	0	1	2	3	4	5	6	7	
Reserve light Off	0	0	0	0	1	1	1	0	0
Reserve light On	0	0	0	0	1	1	1	1	1
ECC mode On	0	0	1	0	1	1	1	1	0
ECC mode Off	0	1	1	0	1	1	1	1	1
Read check light On	0	1	0	0	1	1	1	0	1

The control instruction provides the ability to control the card reader with the main program. The reserve light on or off permits the programmer to signal that the card reader is reserved (or not reserved) during a program run. The ECC mode On or Off permits the programmer to alter from non-ECC mode to ECC mode and back again when required. The read check light is a control function used to indicate that a data error has occurred.

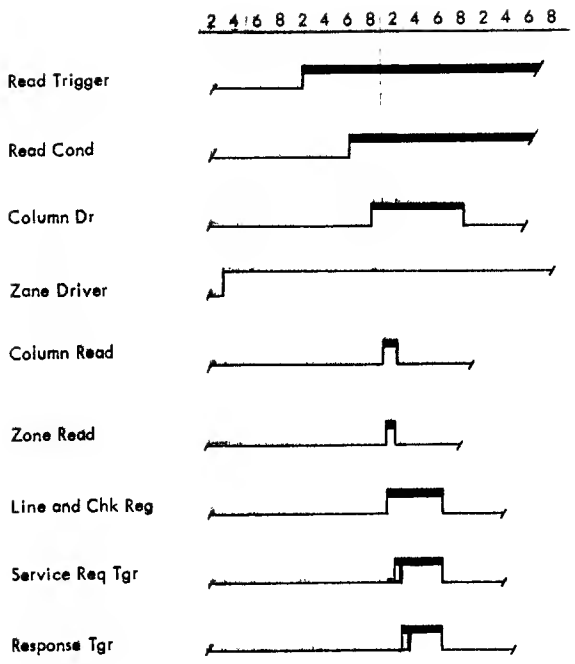


FIGURE 6.3-2. CARD READER, READ SEQUENCE

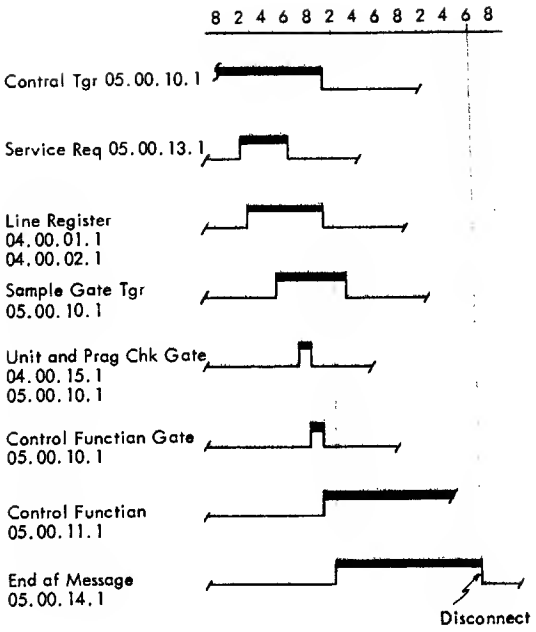


FIGURE 6.4-1. CARD READER - CONTROL SEQUENCE

Figure 6.4-1 is a flow chart of the control operation. A control signal from the exchange turns on the control trigger to initiate a control function. At clock 2 time the service request trigger is turned on and the service request signal to the exchange initiates the transfer of the function code into the line register. This function code is provided with a parity bit (if the function code is even) and is checked at the reader control unit parity circuit. If the parity check is satisfied, the function code is decoded to energize the proper function line.

The input to the control decode circuit is ANDed with the not-program-check and not-unit-check lines. Because either program or unit check is sensed before the control function output line is active, either of these two error checks prevents a control function. At clock 1 time of the next clock cycle, the sample gate turns on the end-of-message trigger and resets the control operation. Figure 6.4-2 is a sequence chart of the control operation. This chart shows the relation between the functional units during a control operation.

6.5 ECC MODE READ OPERATION

The reader control unit contains the necessary circuits to read IBM cards that are punched in ECC mode (Systems 05.00.12.1). When the cards are punched in ECC mode, six consecutive card columns define one data word. Nine eight-bit bytes are required to transfer this 72-bit data word. (The data word is composed of an eight-bit error checking and correction code and 64 data bits.) The ECC card contains a maximum of 13 data words in card columns 1 to 78. Columns 79 and 80 are not used.

The reader control unit is normally in a non-ECC mode and must be programmed to the ECC mode. The ECC bits assigned to the data words in the card permit automatic single-error correction at the exchange. The ECC mode of operation of the reader control will detect a single error within one data word but will not indicate this error. Double errors within one data word, however, will be detected and will turn on the unit check error.

A control instruction specifying the ECC mode must precede a read instruction in which ECC cards are to be read. When the reader control is altered to the ECC mode, it:

1. provides a constant gate to the input and reset of the trap register triggers,

2. conditions the multiple error circuits so that a single error is detected and a multiple error turns ON the unit check trigger,

3. blocks a single compare error from turning ON the unit check trigger,

4. conditions the turn-on of the early disconnect trigger at column 10, zone 10 of buffer read-out (card column 79),

5. signals the exchange that card reader operation is in the ECC mode.

The ECC trigger +P line to the trap register(Systems 04.00.01.1)at the +OR block 4A maintains a constant input gate to the trap register. The output of block 4A is also used as a constant gate to the trap register reset circuit (Systems 04.00.09.1 - block 3D). Thus, the trap register accepts any error bit at clock 2 pulse of a byte cycle and is reset at clock 6 pulse of the same cycle.

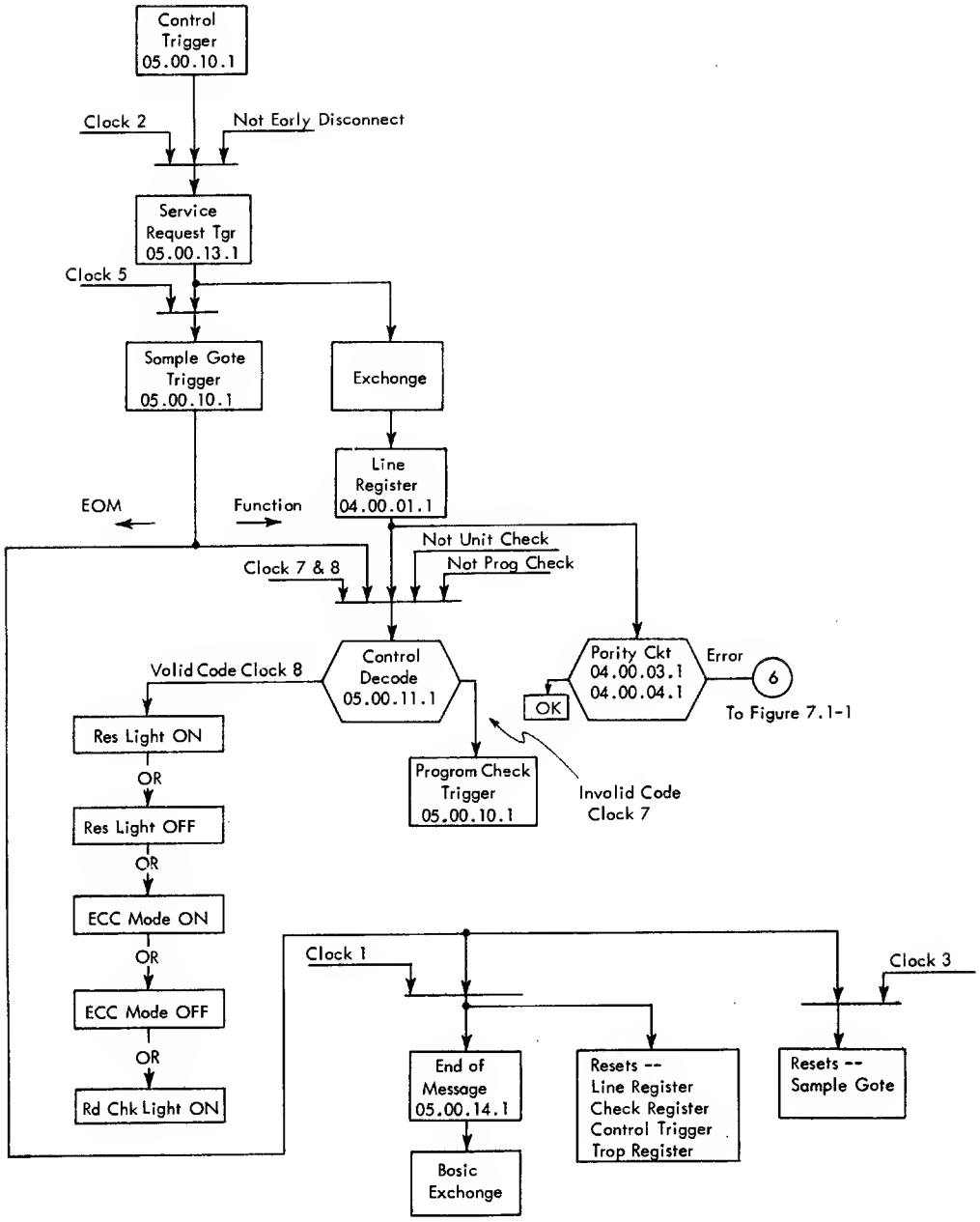


FIGURE 6.4-2. CARD READER, CONTROL FUNCTION

The +N ECC line to the multiple error circuit (Systems 04.00.12.1) activates the multiple-error check during an ECC mode read operation. The error circuit can detect a single error condition and turn on the unit check trigger when multiple errors are detected during one data word transmission (nine bytes per word). While the multiple error circuit is active, the single-error compare circuit is prevented from turning on the unit check trigger (Systems 04.00.15.1).

The data word consists of 72 bits or 9 bytes when in ECC mode. Consequently, the maximum number of words that can be punched into a card is 13. Only 78 card columns are required to punch these words in a card. Thus, the end of a read operation is signalled at column 10, zone 10, and an early disconnect is initiated. The exchange is also signalled that the card reader is in the ECC mode. The exchange, thus, alters its data reception so that nine bytes are recognized as a data word.

6.6 UNLOAD OPERATION

The unload operation (Systems 05.00.01.1) is started by depressing the unload key. However, certain conditions must be satisfied before the unload key is operable. These conditions are: (a) cards cannot be in the hopper, and (b) the ready line must be inactive. Hence, the stop key must be depressed and the hopper emptied prior to depressing the unload key. This operation permits the removal of any cards in the reader without reading the cards.

The depression of the unload key causes the following functions:

	Systems
1. Activates partial machine reset.	05.00.09.1
2. Prevents the brush drivers from turning on.	03.00.05.1
3. Turns on the driver trigger to energize the drive motor.	05.00.04.1
4. Turns on the clutch trigger to energize the card feed clutch.	05.00.04.1
5. Prevents the start trigger from turning on.	05.00.06.1

During the unload operation, the reset does not affect a reset on the control functions which are program controlled. Further, the clutch drive trigger and unload trigger are not reset by the unload reset.

6.7 OUT-OF-MATERIAL OPERATION

An out-of-material light indicates that the stacker is full or that the last card has fed from the hopper. When the stacker switch activates the end-exception condition, the end-exception trigger is not turned on until the following read operation is terminated. Hence, the data of the card that transfers the stacker switch are transmitted to the exchange before the out-of-material light is illuminated. In the second instance, when the hopper runs out of cards, three subsequent read operations (two card feed cycles) occur before the out-of-material indication is given. The card reader is emptied of cards, in the latter case. Thus, the data of the last card in the stacker are transmitted before either situation turns on the end-exception trigger.

Cards should not be loaded into the hopper of the card reader once the hopper empties, because the exact location of the last card in the reader is not discernible. By placing cards in the hopper before the previous cards are completely read and run out may result in a feed check condition. This feed check condition would result if a card were at the

second read station when cards are placed in the hopper. The subsequent card feed cycle would sense the absence of cards of the first read station and give a feed check indication.

An end-exception bit is set in the reader control word at the end of the operation. Systems 05.00.08.1 contains the circuits for the end-exception detection. AND block 5B senses the absence of cards in the hopper, and AND block 5C detects a full stacker condition. In either case, the carry trigger ON level must be present before an output to the end-exception trigger is permissible.

AND block 5B input is conditioned with a +N line when card lever 1 is not made. This block permits a single-card feed and read operation.

6.8 DISCONNECT FUNCTION

The disconnect function is initiated by a release instruction or when a reader operation is terminated. Normally, the disconnect signal is supplied by the exchange; but, if the reader is in a test operation, the test disconnect trigger within the reader control unit starts the disconnect. In either a normal or test situation, the end-of-message signal begins the disconnect function. The card reader control unit, however, is disconnected at any time during a reader operation by a programmed release instruction.

This disconnect function resets the following triggers which were set to define the operation in the reader control unit, end-of-message trigger, cancel trigger, single-error trigger, single-error gate trigger, and channel signal trigger.

In addition, if the disconnect signal is activated during a read operation by the release instruction or a cancel signal, the disconnect signal turns on the early disconnect trigger. This early disconnect trigger interrupts the transmission of data to the basic exchange. The functions controlled by this trigger are:

1. Block the service request trigger to prevent data transmission.

2. Start the go clock trigger to continue the 8 stage clock operation.

3. Block the multiple error circuit.

The early disconnect function is activated before the data of the current cycle are completely transferred. Consequently, the eight-stage clock continues to cycle, and provides a flushing operation to empty the remaining data in the buffer. At the end of the buffer read-out, the 120th byte signal begins the normal end-of-message operation to indicate that the operation in error is complete.

The cancel signal is turned on in the reader control unit by any one of three check circuits. These checks are: ring check, driver check, or feed check. Whenever one of these checks is activated, the current data are considered as completely invalid. Consequently, the cancel signal to the exchange initiates a disconnect and stops data transmission. The subsequent disconnect signal to the reader control unit turns on the early disconnect trigger to terminate data transfer.

When the reader control unit is in a test status, the end-of-message (EOM) signal is blocked from the exchange. However, this EOM signal turns on the test disconnect

trigger, and internally starts a reader control unit disconnect. Figure 6.8-1 is a flow chart representation of the disconnect function. This disconnect function in the reader control unit is activated internally or from the basic exchange. This is shown in the flow diagram with the Systems number of each block representation.

6.9 CHANNEL SIGNAL

The channel signal (Systems 05.00.06.1) provides communication between the operator at the card reader and the computer. This signal is used through the machine program to request a read operation or for the initial program load operation. The channel signal is activated when the card reader is initially placed in a ready status or when the channel signal key is depressed. The channel signal indicator is set in the channel control word immediately if the reader is not being used. However, if the reader is in an operation, the channel signal indication is not transferred to the indicator register until the operation is completed.

When the card reader is initially loaded and run-in, the prepare ready trigger (blocks 4B and 4C, Systems 05.00.06.1) is turned on. The prepare ready trigger turns on the ready trigger and the outputs of these triggers are ANDed with the signal key line (+) and clock 7 pulse (block 3A) to turn on the channel signal trigger. The channel signal trigger turn-on resets the prepare ready trigger, and the channel signal trigger is reset by a disconnect. The prepare ready trigger remains off until the ready trigger is off during a clutch cycle. The prepare ready trigger remains off because the +AND input (block 5B and 5C) to this trigger is conditioned by a +not-ready line. Consequently, the channel signal is automatically turned on for the initial run-in operation only.

The channel signal, however, may be turned on at any time while the reader control unit is in a ready status by depressing the channel signal key on the card reader. This key results in turning on the prepare ready trigger. When the key is released, the channel signal trigger turns on. The line from the signal key is normally a plus level, but goes to a minus level upon key depression. Thus, the input to block 4A goes minus when the key is depressed and block 4A output rises to a plus level to turn on the prepare ready trigger. Because the key line is minus while the key is depressed, the output of the AND block at 3A is not active (minus level). However, this output line goes plus as the key is released and, because the prepare ready trigger is on, the output of block 3A is plus and the channel signal trigger is turned on.

6.10 MULTIPLE ERROR CIRCUIT

The multiple error circuit (Systems 04.00.12.1) is conditioned to function when the reader control unit is in an ECC mode of operation. This circuit is designed to detect multiple errors in one data word. Because data are handled in bytes, the possibility of multiple errors in one byte is also detectable. Single errors within one data word are detected but an error indication is not activated. The reason is that the ECC code assigned to each data word will automatically correct a single data error. Because the error detection is on a word-by-word basis, the multiple error detection circuit is reset at the beginning of each data word. The byte 9 counter generates the reset pulse at the beginning of each data word to be transmitted. Hence, the multiple error circuit is conditioned anew for each data word. This procedure is required to prevent the carry-over of a single-error detection in one word to the succeeding data word.

The byte 9 counter consists of ANDing the zone ring triggers output and the column read pulse (clock 1 pulse). This ANDing is provided at byte 1, byte 10, and every succeeding

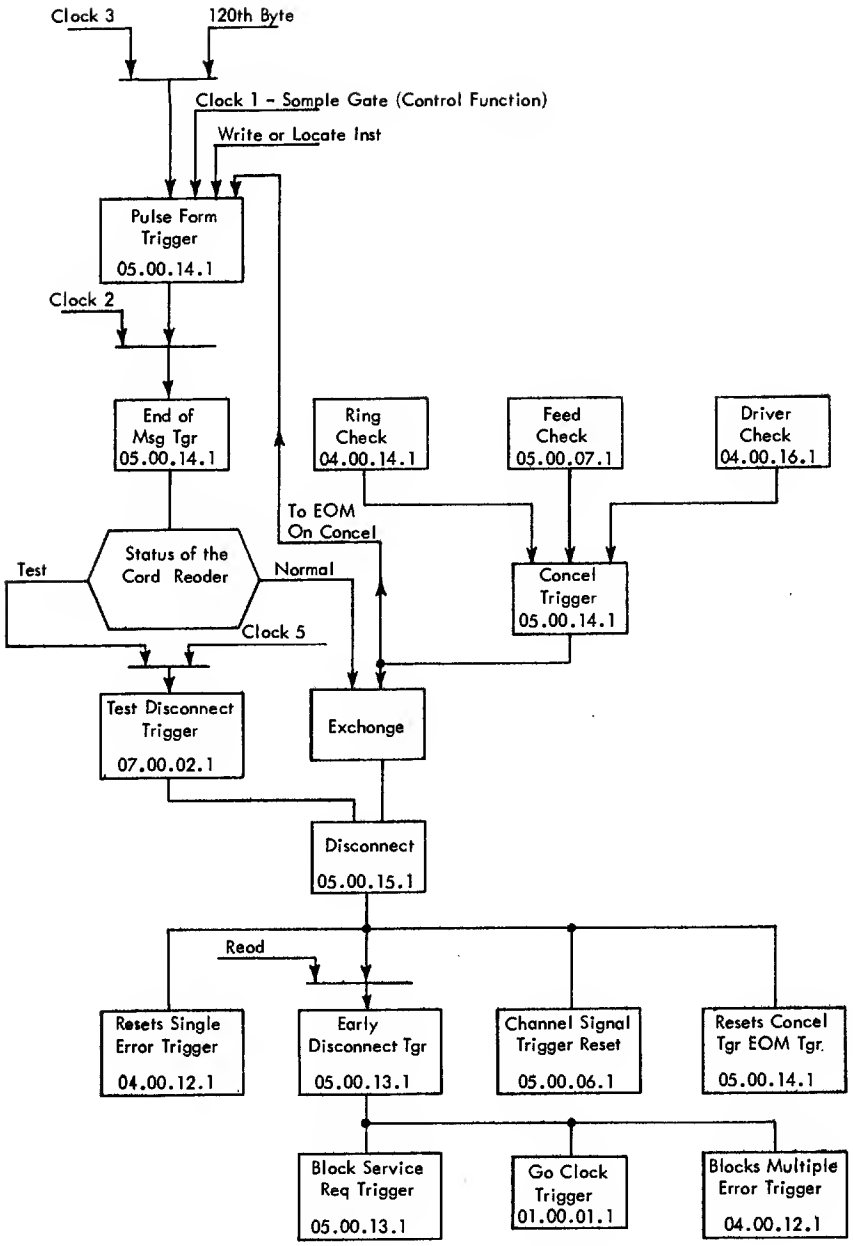


FIGURE 6.8-1. CARD READER, DISCONNECT

ninth byte at clock 1 time. Thus, a zone 1 trigger and column 1 read pulse reset the multiple error circuit for the first data word. This byte 9 counter is located on Systems 03.00.17.1.

The multiple error circuit on Systems 04.00.12.1 is explained as follows: the ECC mode trigger is activated and the +AND block at 3G is supplying an out-of-phase output to condition the multiple error circuit. The output from 3G conditions one input of the -AND blocks at 2G and 2E. The second input to block 2C is provided from the +OR blocks at 4A, B, C, D, E, and 4F. The inputs to these +OR blocks are the data bits of each byte gated at the trap register (Systems 04.00.10.1 and 04.00.11.1). The +OR blocks at 4A, B, C, D, E and 4F detect a multiple error within one byte. Various bit combinations are provided to the inputs to these blocks and their outputs are parity-checked at the +AND blocks at 3A, 3C, and 3E. Any output from the +AND blocks (3A, C, or E) results in a multiple-error indication at block 1D.

A single error is detected at the -OR block 3F. A minus output from this block will result in an output at the -A block 2E (second input to 2E is conditioned by ECC mode), and, therefore, at block 1E, also. The in-phase output of block 1E (+) turns on the single-error gate trigger, and the out-of-phase line is used as an input to block 2D. When the first single error in a data word is detected, the input at pin D to the block 2D is plus and the output of block 2D remains inactive. However, at clock 4 pulse after the first error detection (clock 2), the single-error trigger is turned on from the +AND block 3H. The out-of-phase line from pin H of block 2I (single-error trigger) is wired to block 2D, and this block is conditioned to activate an error condition if a second single error is detected within the data word. However, if no further errors are detected (single error), the byte 9 counter output at the beginning of the next data word resets the single error gate and single error triggers. Thus, the multiple error circuit is reset for the next data word checking.

6.11 RESET OPERATION

The reset operation functions to establish the machine circuits to an initial starting status. There are four lines that activate a reset; three of these lines provide reset line levels throughout the machine and the fourth (unload reset) provides a limited reset operation. Systems 05.00.09.1 contains the distributive circuits for a reset operation and the lines that activate the reset. These inputs to the reset circuit are: power on reset, machine reset key, basic exchange reset, unload operation reset. The machine reset key, power on reset, and the exchange reset initiate a complete machine reset operation. The unload reset line does not reset the control functions (such as reserve light trigger, ECC mode trigger and so forth) and the clutch trigger, drive trigger, or unload trigger. The lines on the right of the Systems indicate the gates and triggers to which each line is connected.

6.12 HAYDON TIMER CONTROL

The Haydon timer is an adjustable timer that controls the card reader drive motor. The Haydon timer consists of an electric clock motor that transfers a set of contacts after the elapse of a preset time interval. This timer stops the card reader drive motor if the card reader does not receive a read instruction from the computer for a time interval set on the timer. The time interval is adjustable from two to twelve minutes.

The AND block 5H on Systems 03.00.04.1 controls the Haydon timer. The three inputs to this AND block are: not-gate timer trigger, drive trigger, and not-read trigger. The coincidence of these inputs provides an output to the Haydon timer. If these inputs remain at their plus levels for the time interval set on the timer, the drive motor is stopped.

7 CHECKING CIRCUITS OPERATION

THE INTERNAL check circuits in the reader control unit provide functional and data transmission reliability. These circuits function in three different formats, and each format is determined by the type of error detected. These check circuits and their formats are explained in the following sections.

7.1 UNIT CHECK

This check circuit (Systems 04.00.15.1) monitors data transmission. When a unit check error is indicated, the data transmission is not interrupted, but the current operation is terminated at the end of the block of data in which the error is sensed.

Figure 7.1-1 shows the condition that turns on the unit check trigger and the resultant effect of this trigger. The unit check is turned on by:

1. A multiple error that may be encountered when the reader control unit is in the ECC mode of operation.

2. A parity error that may be sensed in the control code received because of a control instruction.

3. A compare error that may be sensed during a read operation as data are transmitted to the exchange.

The data transfer to the exchange is not interrupted by the unit check. However, the following conditions occur when the unit check trigger is turned on:

1. The byte counter input is blocked to prevent the counter from accumulating after a unit check is recognized; the amount in the byte counter indicates in which byte the data error occurred.

2. The ring check circuit is blocked because the byte counter is made inactive.

3. The sample decode pulse is blocked to prevent a functional control operation from occurring when a parity error is encountered in the control code.

4. The trap register input is blocked and the data bit that is in error is retained in the trap register; if the reader control is in ECC mode, the trap register is not effected by the unit check.

5. The response trigger is reset if the unit check is sensed if the reader control is in test mode (CE test panel operation).

6. The unit check indication is sent to the exchange where the unit check status bit is set in the control word at the end of the current block of data. This unit check line to the exchange, accompanied by the end of message, indicates that the current block contained a data error.

The program uses the combination of the status indicators to determine the disposition of these data.

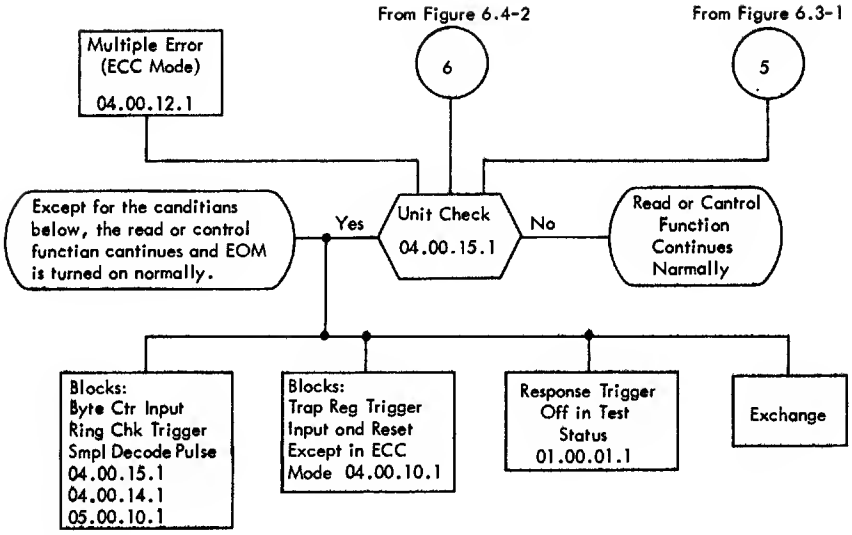


FIGURE 7.1-1. CARD READER, UNIT CHECK

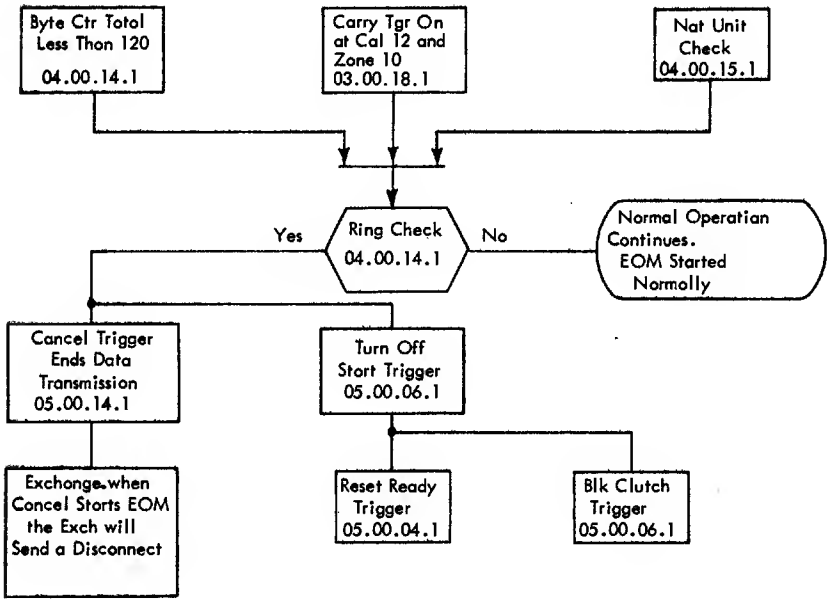


FIGURE 7.2-1. CARD READER - RING CHECK

7.2 RING CHECK

The ring check (Systems 04.00.14.1) interrupts data transmission to the exchange when a zone or column ring error is detected. This check also drops the ready line and initiates a cancel operation to immediately terminate the current read operation.

Figure 7.2-1 indicates the three coincident conditions that must be present to initiate the ring check. During a read operation, as the zone and column rings are stepping to read out the data buffers, the byte counter is pulsed for each byte read. When the zone and column rings reach their last step, the byte counter is sampled for a total of 120. If at this carry pulse (last ring step) time the byte counter value is less than 120, the ring check error is turned on.

When the ring check is detected, the start trigger is reset and the cancel trigger is turned on. Because the start trigger is reset, the ready trigger is reset and the card feed clutch trigger is blocked. Simultaneously, the cancel trigger turns on the end-of-message trigger and an exchange disconnect is initiated. This error indicates a component failure and further operation is prevented. This check circuit is implemented to check that the zone and column drivers do not skip a data byte during read-out. The counter value may be greater than 120 at carry pulse time due to a column's or zone's failure to advance. In this case, the same byte position would be read out twice in succession and the drive check circuit would detect this type of error.

7.3 DRIVER CHECK

The driver check circuit (Systems 04.00.16.1) samples the output of the check cores in the core planes, 1 through 12 during a byte read-out. These check cores are set during a check buffer read-in operation by the row drivers and the pulse power supply (brush driver 2), and are read out by the zone and column drivers. Hence, the driver check must sense an output on the check core sense lines at each byte read-out.

Two core planes in check buffer A and B are addressed to read out by each combination of the zone and column drivers. However, for each read-out combination, one of the check buffers is inhibited. The data bits are inhibited (only) and the check bits in both check buffers read out with each zone and column combination. Hence, for each zone and column combination, eight data bits are read from the record buffer, eight data bits are read from one of the check buffers, and four check bits are read out of the check cores in check buffers A and B.

The check core sense lines are sampled for each byte read-out. Each sense line senses a check core set by one of three row drivers and sets a sense trigger. The four sense lines must set four sense triggers for each byte read out to satisfy the driver check circuit. Figure 7.3-1 shows each sense trigger and the check cores that set the trigger. The output of these triggers are sensed at clock 3 time to determine the driver check. If all the sense triggers are conducting, the check circuit is satisfied and the driver check trigger is blocked. If any sense line does not sense a check core output, the corresponding sense trigger is not set and a driver check ensues.

The driver check, similar to the ring check, initiates an immediate termination of the read operation as follows:

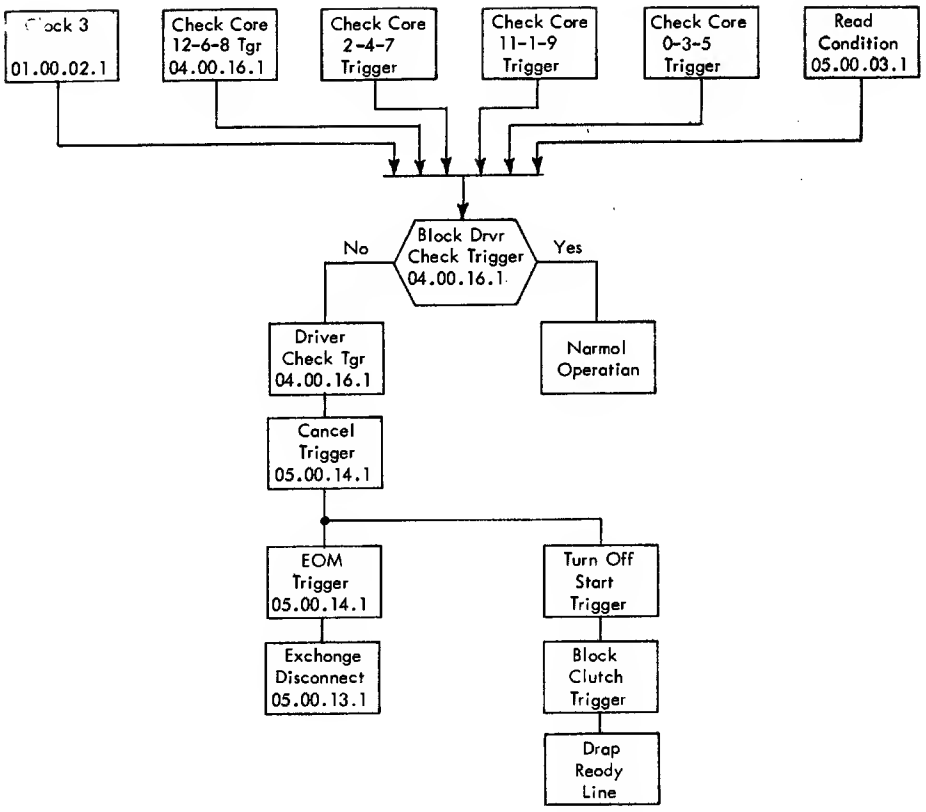


FIGURE 7.3-1. CARD READER DRIVER CHECK

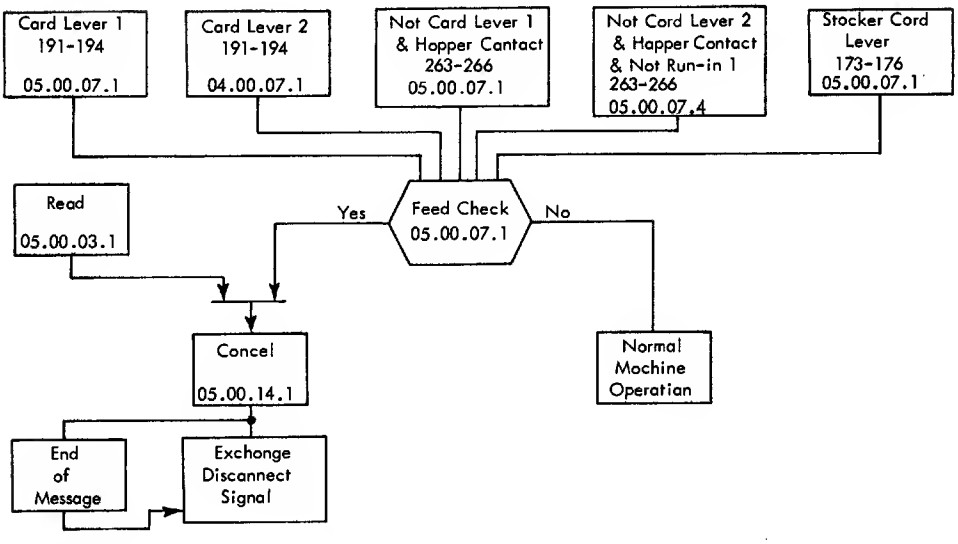


FIGURE 7.4-1. CARD READER, FEED CHECK

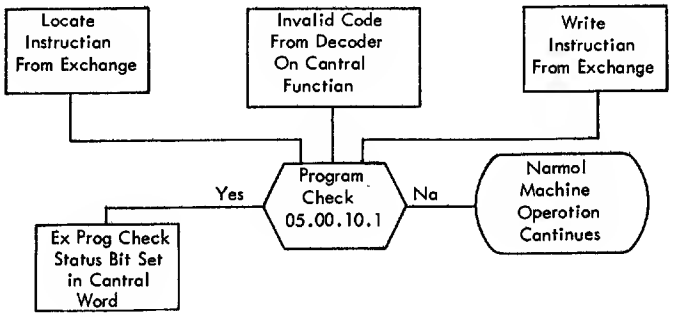


FIGURE 7.5-1. CARD READER, PROGRAM CHECK

1. Sets the cancel trigger.
2. Turns on end-of-message and starts a disconnect from the exchange.
3. Interrupts data transmission.
4. Deactivates the ready line.
5. Stops the clock operation if in error stop while using the CE test panel.

Systems 04.00.16.1 contains the logic for the driver check circuit.

7.4 FEED CHECK

The feed check circuit (Systems 05.00.07.1) monitors the movement of the card through the card reader. When a feed check is sensed, the cancel trigger is turned on and the start trigger is reset. Similar to the driver and ring check, the feed check makes the reader control not ready and initiates a disconnect from the exchange. The feed check occurs during the movement of a card in the reader at which time data transfer is not in progress.

Figure 7.4-1 shows the various card levers and contacts that may turn on the feed check trigger.

Each of the conditions that turns on the feed check is indicated in the respective block. The various card levers and contacts are sampled at specific times in the card feed cycle. Should any of these sample times and contact conditions coincide, the feed check trigger is turned on.

The feed check initiates a cancel and a disconnect from the exchange, and deactivates the ready line. If the feed check is detected during an initial card run-in operation, the ready line to the exchange is not established. In this case the cancel trigger is not turned on.

7.5 PROGRAM CHECK

The program check circuit (Systems 05.00.10.1) tests the validity of the instruction received from the main program or the control function code during a control operation. A write instruction is invalid at the card reader, and because only one card reader is assigned to each reader control unit, the locate instruction is also invalid to the reader channel. Similarly, an invalid control function code, during a control operation, will turn on the program check trigger.

An invalid instruction directed to the card reader will turn on the program check and the end-of-message triggers. If an invalid control function code is detected during a control operation, the control decoder is blocked and the program check trigger is turned on. In either case the reader operation is never started. The program check, associated with the end-of-message trigger, sets the exchange program reject status bit in the control word.

Figure 7.5-1 shows the conditions that may turn on the program check trigger.

8 CE TEST PANEL

THE CE TEST panel provides a central location from which all the card reader operations are similated and tested. When the test panel is placed in test operation, the card reader is disconnected from the computer system. Hence, the card reader is serviceable without interrupting the computer system. Maximum machine utilization is obtained by providing independent I-O test operations.

Figure 8.1-1 is a photograph of the test panel, and shows the names and locations of the indicator lights and switches.

The adjustable bias control for the magnetic emitter pulse amplifier circuits is mounted on the test panel. This control is adjusted to provide a specified pulse width of the magnetic emitter pulses. These pulses are specified for a 500 usec width.

The procedures and operations of the test functions are explained in succeeding sections of this manual.

8.1 CE TEST PANEL SWITCHES

One selector switch, five keys, and nine toggle switches are mounted on the test panel. These switches are described as follows:

Selector switch

The selector switch is a six-position switch that alters the reader control circuits to various test formats.

Normal - allows normal reader to exchange operation.

Test - alters the reader control circuits and divorces the reader from the exchange for testing purposes. In this position, the single byte, unit record, and test control switches are in an operable condition and the card reader is controlled from the test panel. Data are not available to the exchange while in this test procedure. The reader control unit does not stop when an error occurs.

Check Stop - This switch setting is identical to the test operation with the added condition that the reader control stops on an error.

Continuous Run - The continuous run setting permits the card reader to run continuously with one depression of the unit record switch until the cards are run-out of the machine. Data are not sent to the exchange and an error does not stop the operation.

Continuous Run, Error Stop - This switch setting is identical to the continuous run setting. However, an error situation stops the operation at the byte in which the error is detected.

System Test -- This system test operation permits normal card reader to exchange operation with data transfer occurring. However, a unit check or driver check error condition will stop the reader control unit at the byte in error.

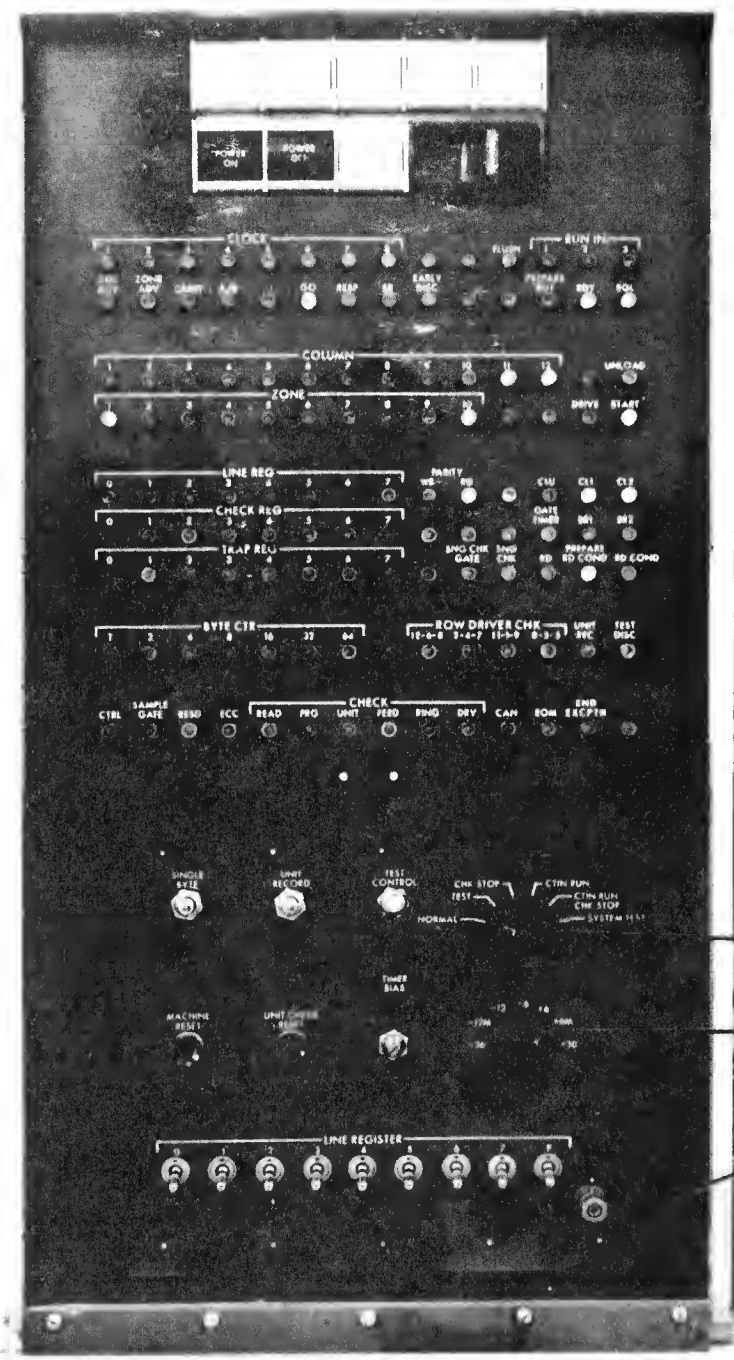


FIGURE 8.1-1. CE TEST PANEL

Keys

Single Byte - With the selector switch in any position except normal or system test, the reader control unit will read out one byte of data from the buffers. The byte is held in the line register and check register at the end of the operation and the contents of these registers are displayed on the lights at the control panel. A carry signal causes a card feed cycle when the 120th byte is read out.

Unit Record - With the selector switch at the test position, the unit record key will read out the buffers and cause a card feed cycle to reload the buffers. When the selector switch is in the check stop position, a unit check or driver check error will stop the read-out. If an error does not occur the read-out continues for one card image and a card feed cycle is initiated at the card reader. When the selector switch is set to continuous run, a depression of the unit record key will result in a continuous card reader operation until the cards are run out of the reader. This operation also results when the selector switch is set to continuous run-error stop with the additional condition that the reader stops on unit check or driver check error.

Test Control - can be started by depressing the test control key. However, certain conditions must be set up before the control operation is initiated. These conditions are:

1. The selector switch is in a test position.
2. A control function code is set in the line register with the bit switches on the test control panel.
3. The test control switch is depressed to turn on the control trigger.
4. The single byte switch is depressed to start the eight stage clock. The clock pulses gate the control operation.

Unit Check Reset - is depressed and the unit check and driver check triggers are reset.

Machine Reset - activates a reset line throughout the machine when this key is depressed.

Toggle Switches

The toggle switches on the test control panel are used to turn on the bit triggers in the line register and the write parity bit trigger. Each bit switch is labeled to indicate the bit trigger that the switch activates. Consequently, any desired bit configuration may be entered into the line register. Whenever a test control operation is performed, these toggle switches must describe a valid control function bit structure. A voltage selection switch and a pair of test jacks are also available on the test panel. The selector switch connects any one of six power supply voltages to the test jacks. A suitable voltmeter is connected to these jacks to read the voltage selected.

8.2 CE TEST PANEL LIGHTS

The various functional units and triggers in the reader control are provided with indicator lamps at the CE test panel. Figure 8.1-1 shows the location and gives the name of these lamps.

These lamps facilitate service procedures and, in conjunction with the test panel switches, provide a visual check of operations. In addition these lamps permit the register to be read and the state of the important triggers to be easily checked.

8.3 SINGLE BYTE TEST OPERATION

The single-byte test operation (Figure 8.3-1) permits a byte of data to read from the record buffer and a check buffer with one depression of the Single Byte key. Several conditions are set before this test is operable. These conditions are: 1) cards loaded and run into the card reader, 2) the selector switch is set to test, and 3) the Single Byte key is depressed.

The record buffer and a check buffer are loaded during the card run-in and, with the selector switch set to test, the data are blocked from being transmitted to the exchange during the test. The selector switch in the test position prevents the service request signal and the end-of-message (EOM) signal from reaching the exchange. Further, this test setting conditions the test disconnect trigger so that the trigger is turned on when the EOM signal is activated. Hence, the selector switch set in the test position isolates the card reader from the exchange and allows the card reader to operate independently. However, all the functions of data transmission are performed within the reader control unit for a single-byte read.

The single-byte test operation initiates the function to read a byte of data from the buffers at the read control unit. The single-byte pulse turns on the read trigger and starts the eight stage clock. With the clock started, a byte of data is read out of the buffers and entered into the line register and the check register. The byte counter is also advanced for each byte read-out operation. When the Single-Byte key is depressed for the 120th byte, the carry trigger is turned on. This carry trigger operation initiates the EOM and, hence, the internal disconnect function.

The single-byte key is designed to provide a pulse output for each depression of the key. A resistor-capacitor network permits the key output to rise to a plus level for a time interval determined by the RC network.

The sequence chart in Figure 8.3-1 shows the single-byte operation. The Single-Byte key turns on the response trigger and the read trigger. These triggers activate only one byte read-out, because the eight stage clock is not permitted to recycle. The clock is started by the response trigger and is turned off at clock 5 ANDed with the service request trigger output. Thus, clock triggers 4 and 5 are on when the clock advance is stopped. A subsequent single byte operation starts the clock from clock 6 and the clock cycles to clock 5. During this clock cycling operation another byte of data is read from the buffers.

The internal check circuits monitor the byte read-out at each depression of the single-byte key. The cancel trigger is turned on when a ring, feed, or driver check is detected. None of these check outputs, including unit check, are accepted by the exchange, because the channel is blocked from the exchange during a test operation.

During the 120th byte operation, the carry trigger is turned on at clock 3 and the read condition trigger is turned off at clock 4. The pulse form trigger is also turned on at clock 3. However, because the service request trigger is on, the clock is stopped at clock 5. Consequently, the EOM trigger cannot be turned on (turns on at clock 2 and

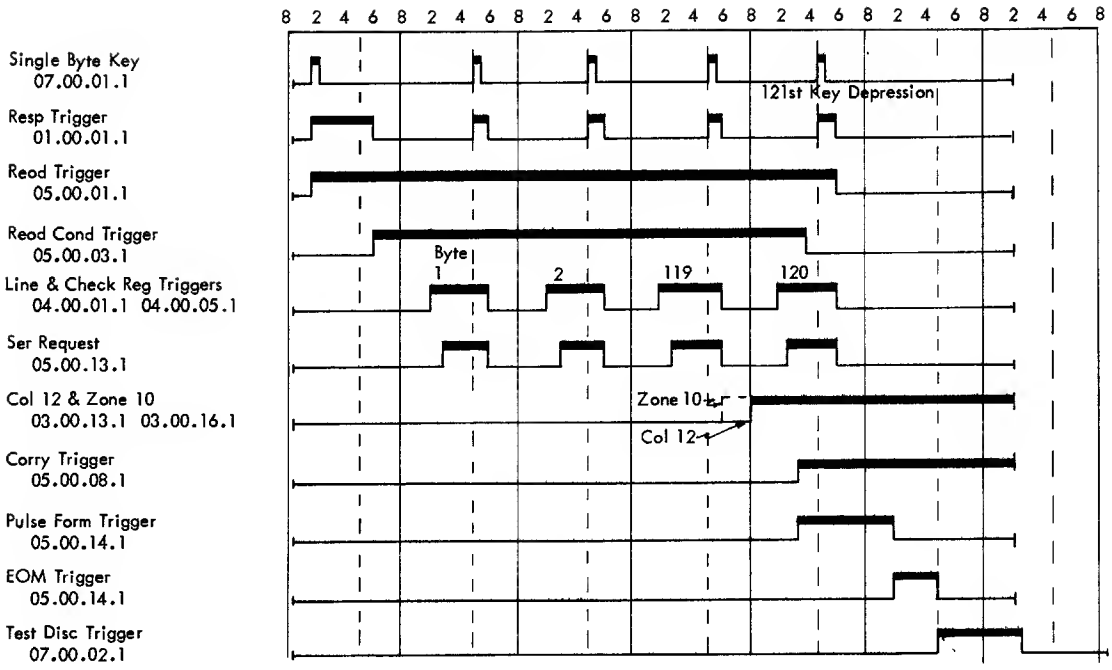
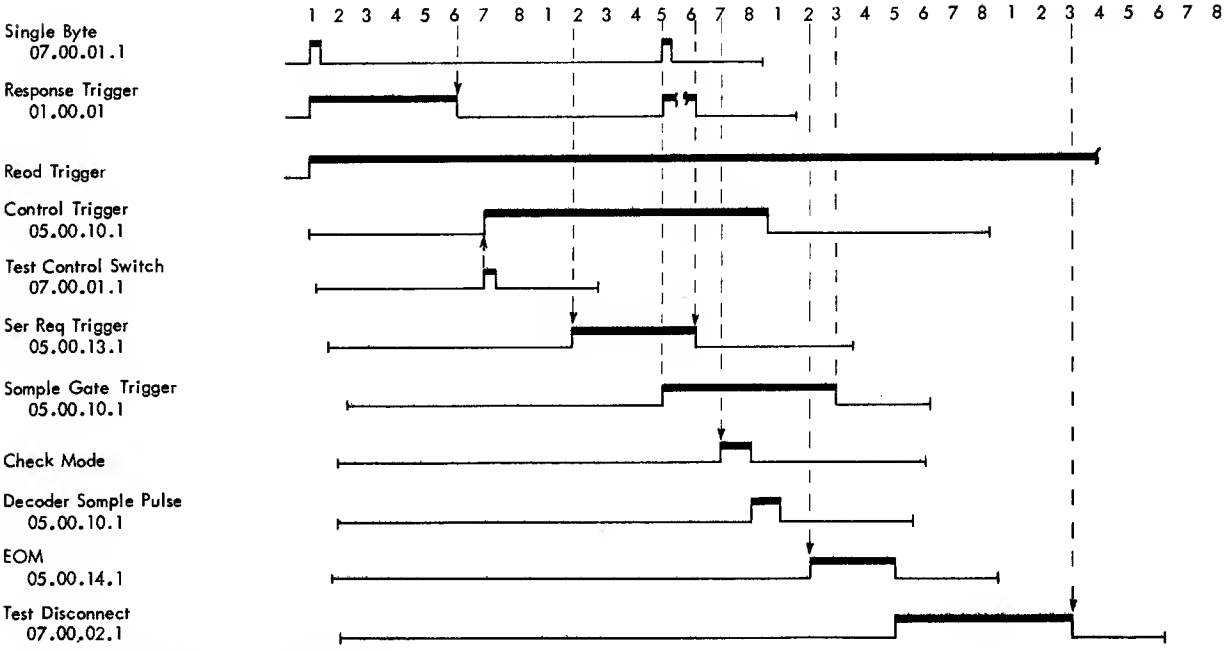


FIGURE 8.3-1. CARD READER, SINGLE BYTE TEST



Note: Clock Stops at Clock 5. Restarted by second depression of single-byte button.

FIGURE 8.5-1. CE TEST PANEL, CONTROL OPERATION

pulse form trigger) until the clock is restarted. A 121st depression of the single-byte key is required to restart the clock. Because the service request is not turned on when the 121st depression is made, the clock recycles continuously. The EOM trigger and the test disconnect trigger are turned on to terminate the single-byte read-out.

When the selector switch is set at error stop, any unit check or driver check error stops the single-byte operation. The situation causing the error is retained when the single byte operation is stopped by an error.

8.4 UNIT RECORD TEST

The unit record test permits a card image to be read out of the record and out of a check buffer when in a test status. At the completion of the buffer read-out, a card feed cycle is started in the card reader. The prescribed conditions are the same as for the single byte test, that is:

1. The card reader is loaded and is in a ready status.
2. The selector switch is in a test status.
3. The unit Record key is depressed.

This unit record operation is similar to the single-byte operation. The main difference is that the unit record test operation reads out the buffers completely with one key depression. The unit record trigger (Systems 07.00.02.1) is turned on by the key and holds the response trigger and read trigger on. The response trigger permits the go clock to run continuously. At carry time, however, the unit record trigger is turned off and the unit record operation is terminated. The selector switch can vary the unit record operation.

8.5 TEST CONTROL OPERATION

The test control circuit implemented in the CE test panel permits a control operation from the panel. For this test control to function, the following conditions must be satisfied:

1. The reader control unit must be not-ready.

2. The line register toggle switches must be set up to a control function configuration.

3. The selector switch must be set to test.

Under these conditions, the single-byte key is depressed to start the go clock operation. When the clock is running, a depression of the test control key and a second depression of the single-byte key starts and completes a control operation.

The sequence chart, Figure 8.5-1, shows the events that occur during a test control. The single byte key initiates the go clock operation. Because the ready line is not active, the read condition and the service request triggers are not turned on. Hence, the go clock is not stopped at clock 5; it is allowed to recycle. With the depression of the test control button, the control trigger is turned on. The first clock 2 pulse after the control trigger is turned on, sets the service request trigger. In test mode, the service request line to the exchange is blocked at clock 5 time; with the service request trigger

on, the clock is stopped and the single byte pushbutton is required to restart the clock. A second depression of the single byte button will again start the clock. The subsequent clock operation will initiate a program check and unit check of the contents of the line register at clock 7. (The line register contents are determined by the line register toggle switches.) At clock 8, the line register is decoded if the checks are satisfied. The following clock 2 pulse turns on the end-of-message trigger and starts the test disconnect to terminate the test control.

9 POWER DISTRIBUTION LAYOUT

THE POWER distribution from the power frame, reader control unit and card reader is shown schematically in Figure 9-1. The power connections are made by two 26-position and two 8-position Burndy connectors within the reader control unit. These connectors are labeled C, D, E and F in the reader control unit, and PP-1 and PP-2 in the card reader. The figure shows the connections and lines between the various units and the terminal board locations. The figure is divided into three sections to show these interconnections.

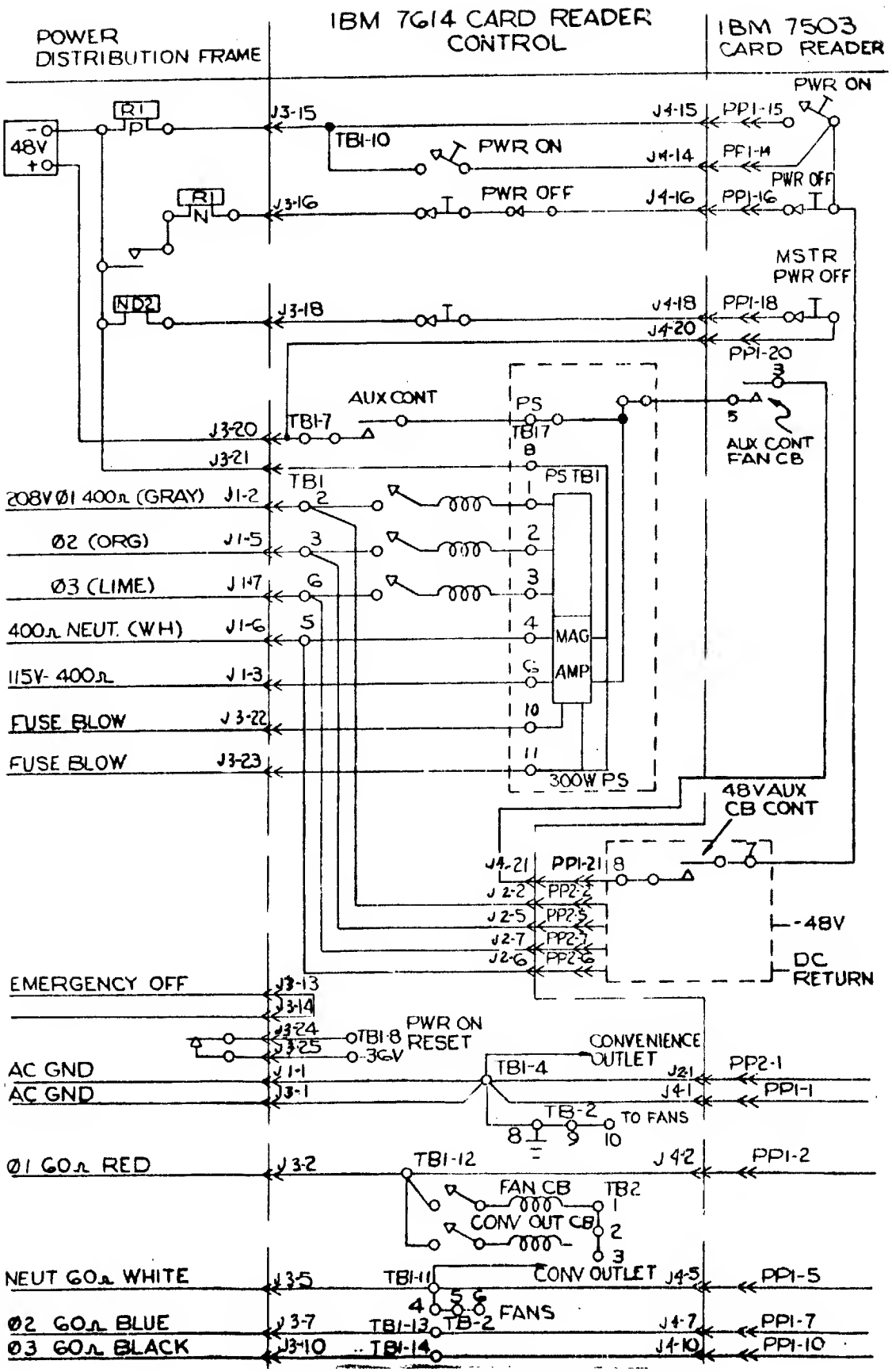


FIGURE 9-1. POWER DISTRIBUTION

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